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FPGA BASED CONDUCTED EMI REDUCTION USING RANDOMIZED MULTISTAGE SIGMA DELTA MODULATOR WITH DECIMATION FILTER FOR DC-DC CONVERTER

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ABSTRACT. Generally randomized pulse width modulation techniques are employed mainly in the protection of power converters from electromagnetic interference and to obtain a large width spectrum with low amplitudes by distribution of the harmonic energy. This paper presents a randomization technique by using high resolution randomized multi stage sigma-delta PWM with decimator (RMSDMD) generation module is implemented for better comparison during the test of conducted EMI noise reduction on DC to DC converter. A unique combination of randomized PWM and sigma-delta concept has been created to overcome problems associated with noise generation. This proposed (RMSDMD) PWM wave generation modules are implemented on an Alter a FPGA device using Quartus II synthesis software tool. Experimental results depict the considerable improvement in the conducted noise spectrum and the noise level was effectively reduced in the range of 9dBμV over other PWM Modulator.

Keywords: Electromagnetic interference, DC-DC Converter, Power spectral density, RPWM, Randomized Sigma–Delta modulation with decimator filter, FPGA.

1. INTRODUCTION

Power electronics plays the major role in the weakening of our electromagnetic environment, affecting the power line quality and conducted electromagnetic interference (EMI),is considerably increased.[1].PWM techniques have been the topic of demanding exploration in the past few decades. The pulse width modulation (PWM) is the widely used technique for controlling DC power to ambiguous electrical devices in sophisticated electronic power switches. The PWM scheme is employed to modulate Switched-Mode DC-DC converters operating in buck mode configuration as shown in Figure1. The use of PWM for MOSFET operation in the buck convertor makes the switching action to be happened more rapidly, thereby resulting in fast transitions at the input current *Vin* drawn by the converter at its node voltageVx.

The input current produces harmonics cause conducted (EMI) noise [2], [3] that passes along PCB traces or power lines and causes interference to neighboring electronic circuits connected to the converter. It is essential to suppress the EMI generated by DC-DC converter as noise-sensitive analog circuits are connected at the identical power line. Many techniques have been used in the past decades to moderate the conducted EMI. When the power transistors transitions

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are slowed down, the high-frequency harmonics are reduced by soft-switching transition techniques [4]–[8. However, the circuit layout design decides the performance level of this approach [6], [9]. Other methods incorporate a devoted spread-spectrum clock generator design for the power supply but the complexity, cost and power consumption are high [10]. Another common approach is employed in origin suppression of the conducted EMI by using spread-spectrum modulation schemes as a substitute of the PWM. The usage of these modulation schemes reduces the peak spectral power of the harmonics by distributing the switching frequency harmonics power over the input current frequency spectrum. This schemes are comes under the randomized category and it may either more than two parameters for modulation whereas to make frequency of switching [11-16] along with PW [12], [17] & [18] for the available frequency for switching includes with PW [19], [20], [21]. However, the scheme which may comes under spread spectrum mode and it is used to modulate the switching level along with some stipulated frequency [22] signal which is used to make a comparison in terms of traditional PWM and it is used to increase the value of noise in low frequency [23], [24]. In this paper, along with a multi-stage decimator filter, a novel sigma-delta modulation is used to combine the randomized modulation scheme and to introduce new circuit design flow techniques along with some other practical examinations have been included. Among the usage of many filters, Multirate filters are used various sampling and its values with respect to various process of filtering stages [24], [25]. The interpolator and decimators have been included along with narrow band frequency with respect to low pass filters which may have direct use of decimation for conventional filtering for low pas signal.

A term modulation is comes under the randomized technique which is used to reduce the switching based frequency and its harmonics alongside with multi-stage has been used to make the noise shaper for the frequency spectrum which has low-frequency noise [26], [27], and the proposed method is being used for oversampling the designed modulators and the operating frequency is relatively low with respect to ratio value of oversampling. Here, a noise value has been decreased further whereas the noise out-of-band might be multiplied for multiple different stages of shaping for SDM noise. However, SDM is referred as most utilize applied method in terms of maintaining accurate ADC of under sampling thin band signals. The uses of ΣΔ ADCs are expanding step by step in various territories like wideband applications, clinical and sound applications. The paper is coordinated like: Section II is directly portrays and it may involves power-circuit plan for converters, sigma-delta spread range plans in converters, simple to circuit by computerized transformation along with required driver. The proposed FPGA-based advanced regulator which incorporates computerized compensator, pseudorandom stream generator, and randomized multi-stage sigma-delta beat width modulator with decimator channel Section III illustrates the trial based test circuit subtleties. In section IV has trial outcomes and its investigation analysis. At last, it has been ended up in area V. FPGA based Randomly Switched Multi-stage Sigma-Delta Modulator along with Decimation Filter for DC-DC buck converter.

1.1 Randomized PWM

The haphazardly switched DC-DC buck converter and its general circuits are being utilized by FPGA. Also, it comprises of power based DC-DC exchanging circuit, sigma-delta ADC circuit and drivers. The proposed system FPGA arbitrarily exchanged Multi-stage sigma-delta modulator with decimation filter based digital regulator, interface and driver for power switches.

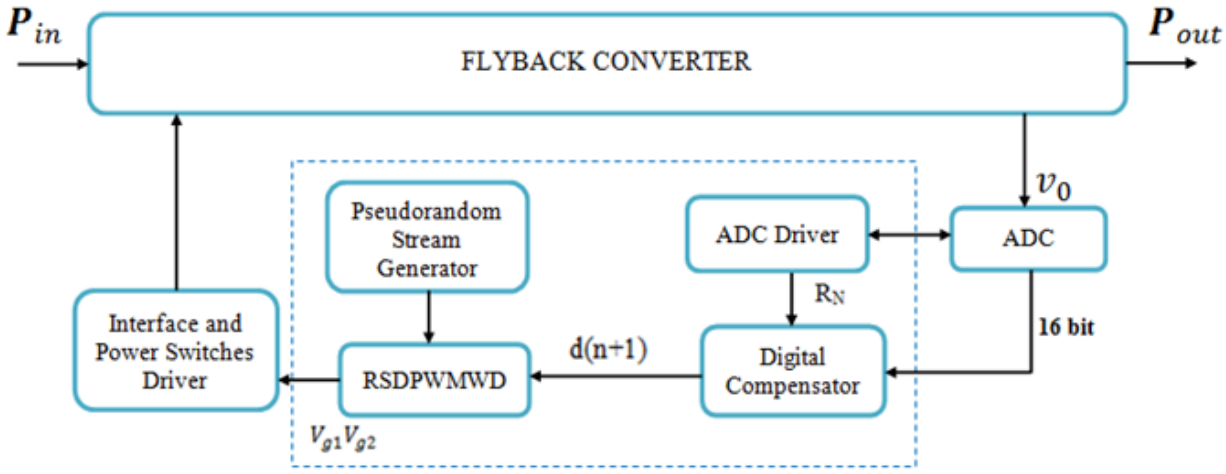

Figure.1 FPGA based digital controller

1.2 Converter Power-Circuit Design

The arbitrarily exchanged DC-DC based converter has been planned and Alter a FPGA is executed and utilized. Asynchronous type buck topology of synchronous duck converter was chosen for enhancing the efficiency whereas to reduce the temperature loss. The resultant inductor and capacitor are estimated with the end goal; however this converter works in a continuous based conduction mode (CCM). The dimension calculation of conduction noise were taken at,

$V_{in} = 12\,V,\ V_o = 5\,V, I_o = 2A$

The Center switching frequency $fcsw = 300\,kHz.$

The spectrum analyzer Resolution band width $RBW = 40kHz.$

The maximum value of ripple voltage should be maintained within $Vr = 20mV.$

Current ripple ratio $r \approx 0.4.$

1.3 Sigma Delta Spread Spectrum Schemes in Converters

The theory illustrated in Figure 2, T_k is a span of the k[th] sequence α_k is the length for ON condition inside this position and ε_k is the deferral by the start for changing position to turn on.

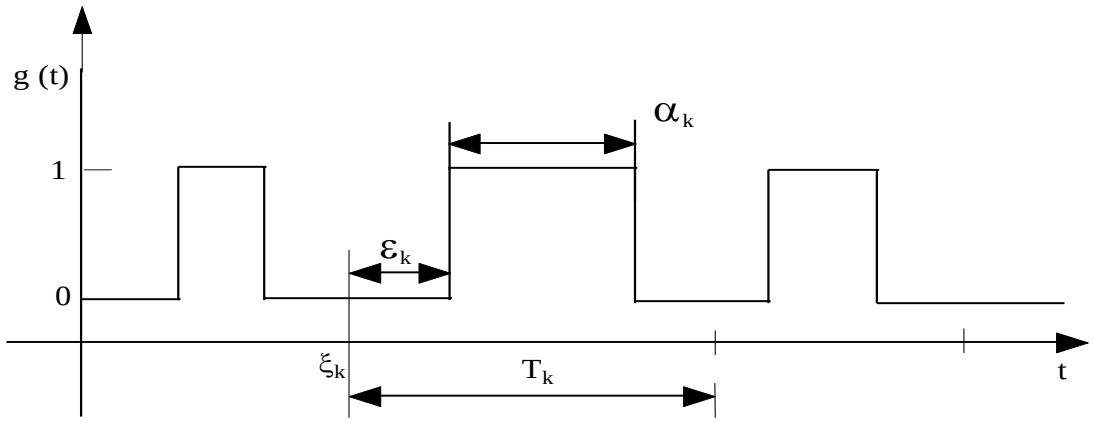

Figure.2 Signal Switching Randomization Parameters

Table.1 Various Schemes Parameters for Randomization

Scheme	R - Parameter			α_k
	F_k	d_k	ε_k	
PWM	Const.	Const.	Const.	Const.
RPWM	Const.	Rand.	Const.	Rand.
RSDPWM	Const.	Rand.	Const.	Rand.
RMSDPWMD	Const.	Rand.	Const.	Rand.

The duty ratio is $d_k = \alpha_k/T_k$, and this frequency of switching is $F_k = 1/T_k$. This type of function $g(t)$may contain of a series of various switching sequence. Before doing randomization it is necessary to transfer the switching noise frequency spectrum, $\{f_k$,$d_k$and $\varepsilon_k\}$. Here Table 1, sums up every one of the potential plans that can be completed for this reason. Several randomization plans utilized in this portion are as per the following:

i. RPWM: $d_k$and α_k changes; $F_k$and $\varepsilon_k$are fixed.

ii. Randomness Levels

To explore the viability of the analytical based variable arbitrariness position in spreading consonant force, an irregularity level R for each plan is characterized,

For RPWM,

$$R_{RPWM} = \frac{\alpha 2 - \alpha 1}{T_s} = d_2 - d_1 \quad (1)$$

Where $\alpha_k = \epsilon[\alpha_1, \alpha_2]$.Hence, the duty sequence$d_k$varies from the low probable value d_1, and the high probable value$d_2$around the predominant duty sequence that is in classical PWM scheme.

1.4 Driver Circuit of ADC

The base converter yield voltage has been changed over into an advanced 16-digit signal by methods for ADC. The sign is performed with the help of computerized compensator whereas to gauge the obligation proportion. This driver is planned and inserted to FPGA-positioned advanced regulator. As demonstrated in Figure. 3, RD is brought low after the rising edge. It used to finishes the change and empowers and the yield supports that contain some transformation outcome. The signal Read Now (RN) has been brought high after finding the falling boundary which may order the computerized compensator to peruse the change in outcome. The transformation sequence is begun along with the exchanging sequence and is finished inside a similar exchanging sequence.

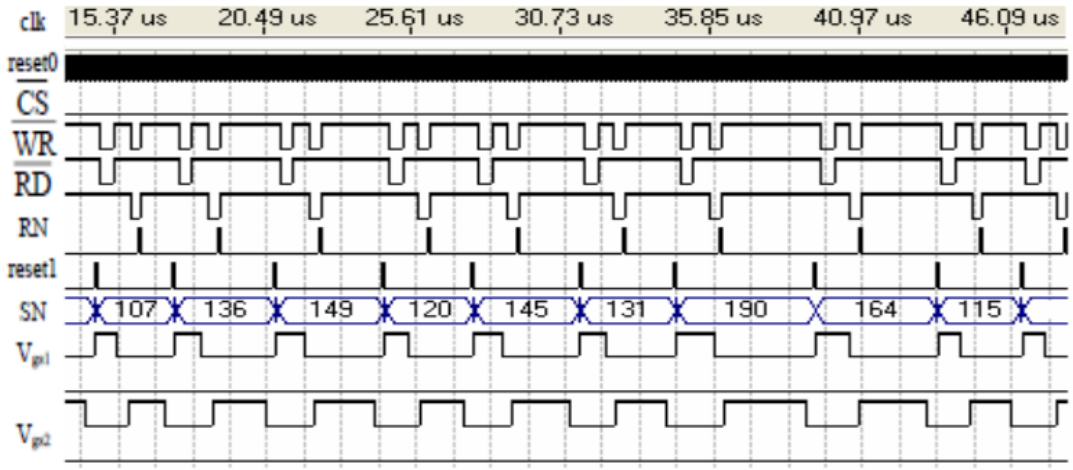

Figure.3 FPGA-based digital controllers and its VHDL simulation outcome

1.5 Digital Compensator

To manage the resultant voltage to coordinate with an exact reference voltage on a range of info voltage esteems, load flows, and heat varieties, an advanced compensator also planned. An advanced compensator creates the yield voltage impervious to its randomized modification in frequency exchanging outcome. As shown in Figure 4, while the input or current exchanging sequence, the computer based compensator ascertains an advanced obligation proportion for the following exchanging sequence. At the point when the yield voltage moves toward the ideal worth, the obligation sequence is frozen. Thusly, a stable working condition is gotten. In this way, the utilization of a no man's land comparator forestalls undesired motions at the converter resultant.

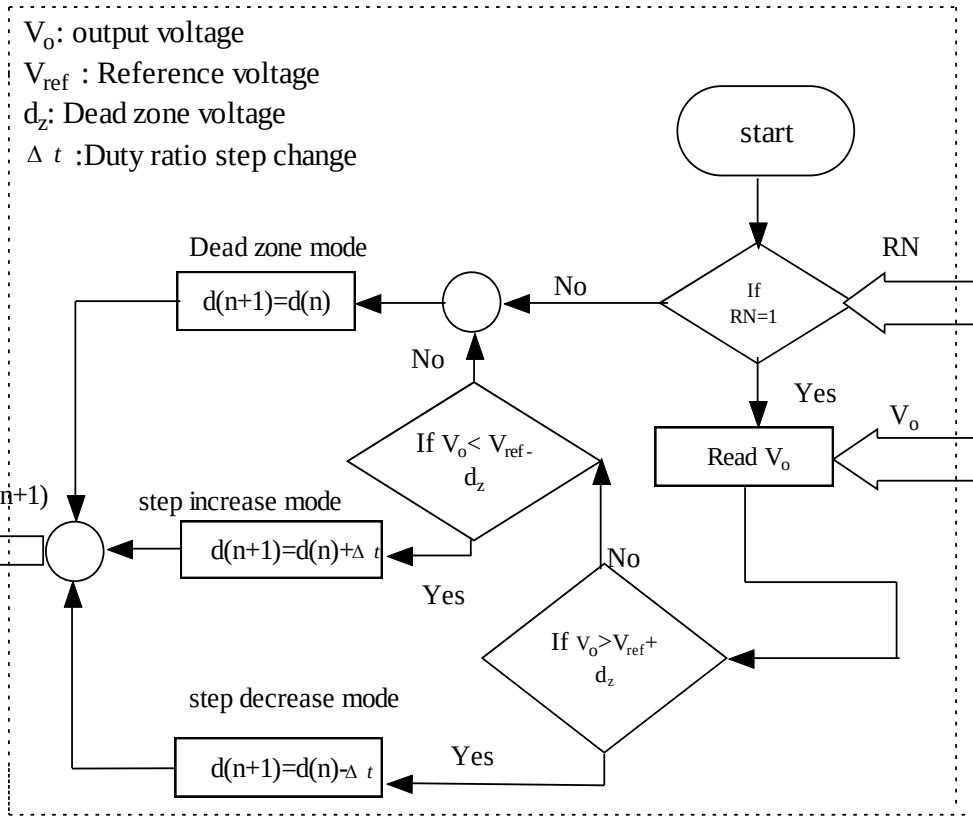

Figure.4 Digital compensator basic flowchart

1.6 Stream Based Pseudorandom Generator

A Pseudo-Random based Number Generator (PRNG) is a Deterministic Random Bit Generator (DRBG) calculation used to create the random numbers with similar properties. These random numbers are not true random numbers since it can also be created utilizing random number generators for specific hardware. Figure 5, illustrates the structure of shift register and its linear feedback.

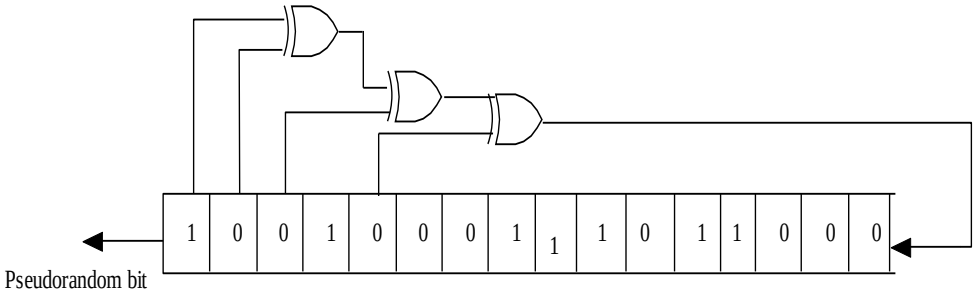

Figure.5 Structure of LFSR

Basic terms of LFSRs are,

(1) Required Registers(R)

It is really based on the integer of letters which is presented in the numbering system. Here, If N is the number of letters and then the R is given by,

$$2^R >= N > 2^{R-1} \quad (2)$$

(2) Equivalent Values

A relevant number is assigned to all letters in the number systems. Ex: ASCII codes are relevant number for ASCII number system.

(3) Seed Sequence

It depends upon the keyword. In which are arranged in FCFS order by eliminating replica is known as seed sequence [28].

(4) Length of Random Number

It depends upon the whole count of necessary exceptional random number and it is calculated by,

$$2^L >= U > 2^{L-1} \quad (3)$$

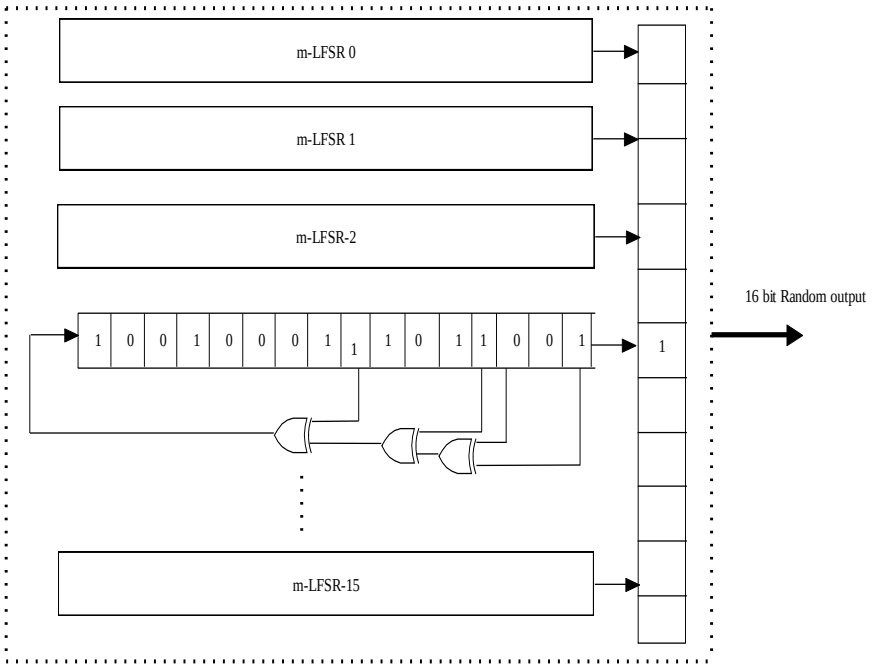

Figure.6 Stream based Pseudo Random Generator basic structure

A PRNG is established from a random preliminary state which produces an identical sequence when started with the same state. The size of the state declares the maximum length of the series. For many practical applications, it is ease to produce long period PRNGs and the greatest period length has been doubled along with every individual bit of 'state' may get

included to respective position of bit. Generally, feedback shift register are used with effortless realization property.

The three parameters and can be randomized by using this pseudo-random generator. This generator is constructed for this purpose in which several maximum-length LFSRs are connected in parallel (m-LSFRs). Different seeds are used for different LFSRs. The taps are XORed and the output is fed back to the LSB which gives three different random streams. All LFSRs are clocked in a sequential manner. Toward the start of each exchanging sequence, these three irregular yields are changed over into number numbers and are utilized in the sigma-delta modulator [29][30]. The planned stream based pseudorandom generator can convey the 16-digit outcome; the higher number it can be created. Toward the start of each exchanging sequence and the DPWM accomplishes its accompanying tasks:

i. Consider the input $d(n+1)$, referred as the duty-ratio of initiated switching sequence $(d(n))$.

ii. Transformation of the output of pseudorandom bits into Integer Number (IN).

iii. Consider the frequency of switching for the initiated sequence and a required clock number (SN)to complete the sequence as follows:

$$F_{SW} = F_L + J * IN \quad (4)$$

$$SN = F_{CLK} / F_{SW} \quad (5)$$

$$DR = SN * d(n) \quad (6)$$

Whereas;

F_{SW} : Switching frequency

F_L : Limit value of Lower frequency

J : Required amount of frequency randomization and constant range

IN : Transforming Pseudorandom Output Stream Integer Number

SW : Switching Frequency Required Number of sequence

F_{CLK} : Frequency of System Clock

DR : Desirable Number of Steps to Complete the Duty-ratio

DS : Quiet Time

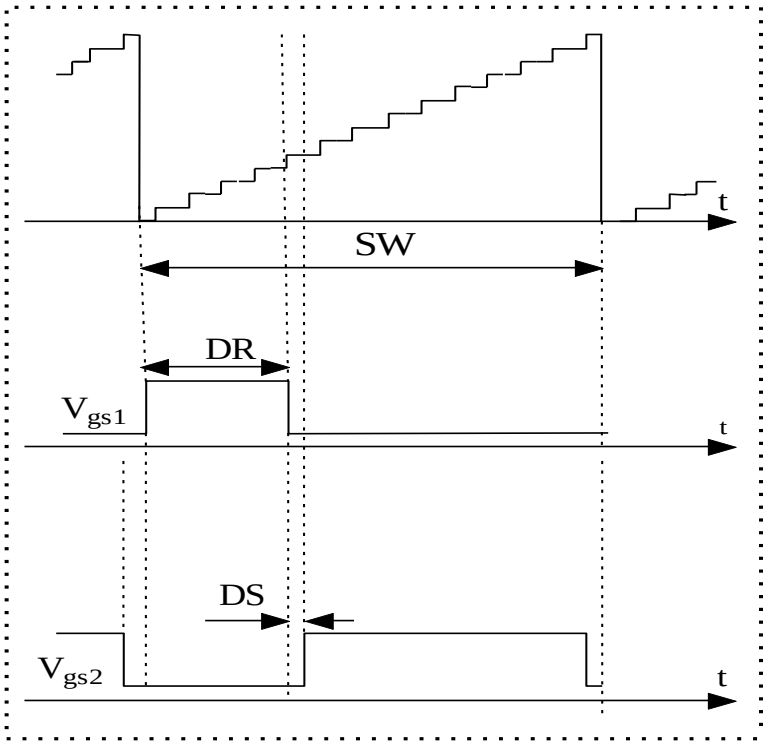

Figure.7 Gate signal generation using DPWM

The entry level of each switching sequence where as the transformation of randomized bits into IN and are applied to multi-stage SDM with decimator filter (RMSDMD) and it will generate the gate signal (AND) as shown in Figure 7. Here SW – number of steps expected to satisfy the exchanging recurrence, DR-number of steps expected to satisfy the obligation proportion, DS - number of steps expected to satisfy the beat position. The planned multi-stage based irregular modulator utilizes timed counter that increments up to the following exchanging sequence SW and reset toward the finish of the exchanging portion as shown in Figure 7.

2. THE PROPOSED MODEL WITH FOURTH ORDER RANDOMIZED MULTI-STAGE SIGMA-DELTA MODULATOR WITH DECIMATOR FILTER

2.1 Revisiting Sigma-Delta ADC with a Novel Approach

The sigma-delta ADC is ideal for low-to-medium speed and high-goal applications contrasted with different sorts of ADCs.ADC capacities as an interface between the simple universe of sensors and the advanced universe of information giving and sign handling. Test and hold circuits, quantization, and encoding are the two critical strides in any ADC module. Commonplace sigma-delta ADC would contain a sigma-delta modulator followed by a low-pass channel. The ΣΔ ADCs operation on the rule and information signal has been oversampled and the noise quantization can be formed which can be eliminated by advanced channels [31]. A ΣΔ modulator has 3 significant portions, represented in Figure 8.

- A loop filter $H(z)$
- Internal quantization
- A feedback DAC

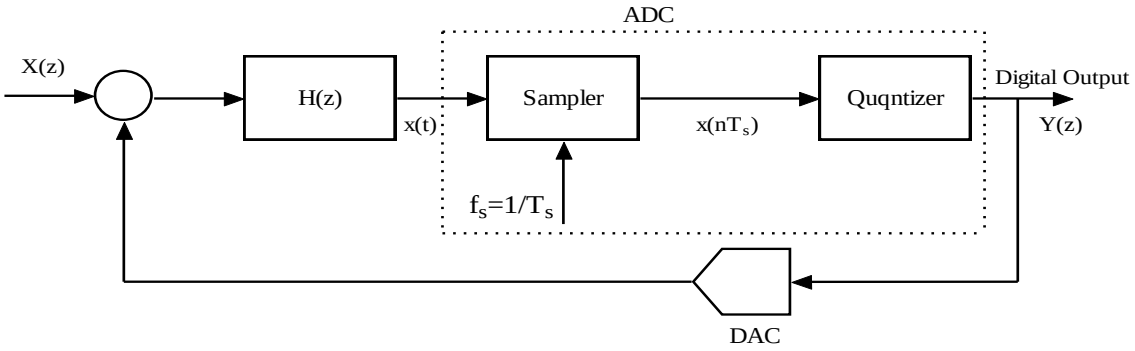

Figure.8 Structure of sigma delta modulator

Hence, quantizer may be type of single or multiple bit operators and it has a strong non-linear based element whereas in single-bit it makes an accurate framework much complex in terms of analytically. However, this linearized framework is illustrated in Figure 9, here the quantizer can be substituted with a basic adder along with quantization based additive noise.

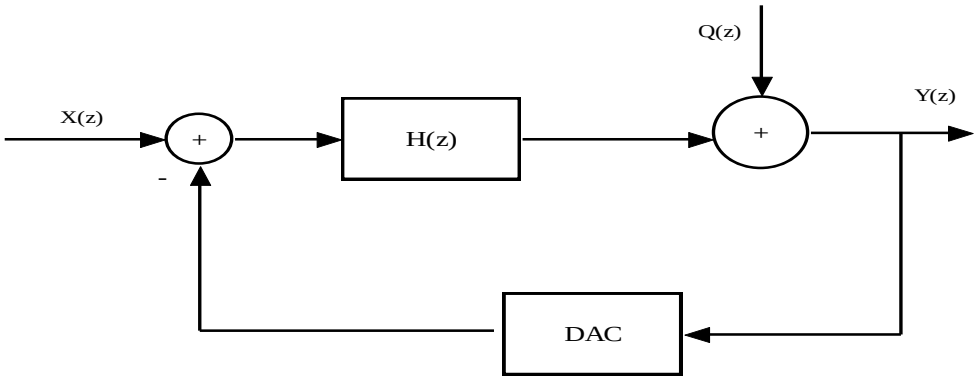

Figure.9 Linearized model of Sigma delta modulator

The outcome is considered as input function and the quantization noise Q(z)with first order ΣΔ modulator equation is given as,

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z) = STF(z).X(z) + NTF(z).Q(z) \quad (7)$$

$$H(z) = \frac{z^{-1}}{1-z^{-1}} \quad (8)$$

by substituting *H(z)* in equation 7,

$STF(z) = z^{-1}$ and $NTF\ (Z) = 1 - z^{-1}$

Therefore,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \quad (9)$$

In the second order case, the transfer function can be written as,

$$STF(z) = z^{-2} \text{ and } NTF(z) = (1 - z^{-1})^2 \quad (10)$$

However, modulators with this type of topology suffer from stability problems to overcome this issue; the higher-order MASH configuration can be used. Where, equation 10 represents the different transfer functions like; single and noise, respectively. Figure 10, illustrates the basic architecture with a decimation filter. To begin this model, this analog signal is being sampled to achieve the discrete time signal. This signal has been deducted by the simple outcome of bit DAC, changing over the m-piece oversampled advanced framework. At that point the thing that matters is shipped off the discrete time simple integrator, which is carried out by the exchanged capacitor method, for instance. A discrete time simple integrator outcome is modified over utilizing an m-piece ADC to create an oversampled computerized signal. At last, the annihilation sift eliminates through band quantization clamor. Further pulverization sequences might have been changed the oversampling value to the ideal testing value for an outcome of advanced framework. The annihilation proportion can be determined by the accompanying equation,

$$Decimaion\ Ratio = \frac{Sampling\ Rate\ (F_s)}{Data\ Rate(F_d)}$$

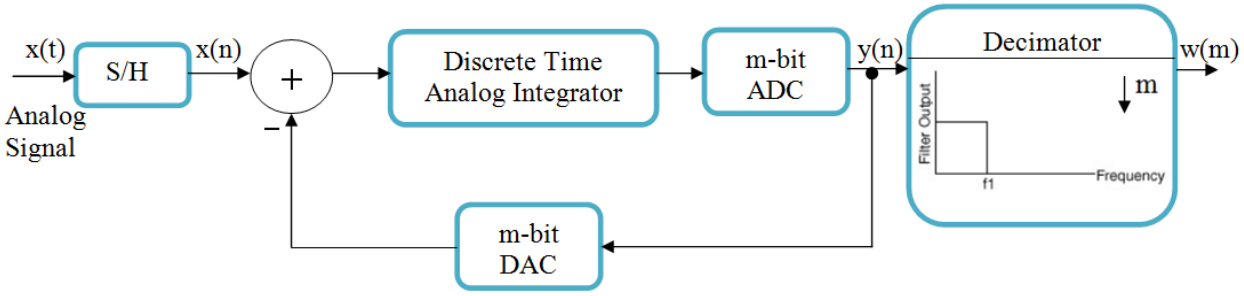

Figure.10 Basic block diagram of $\sum\Delta$

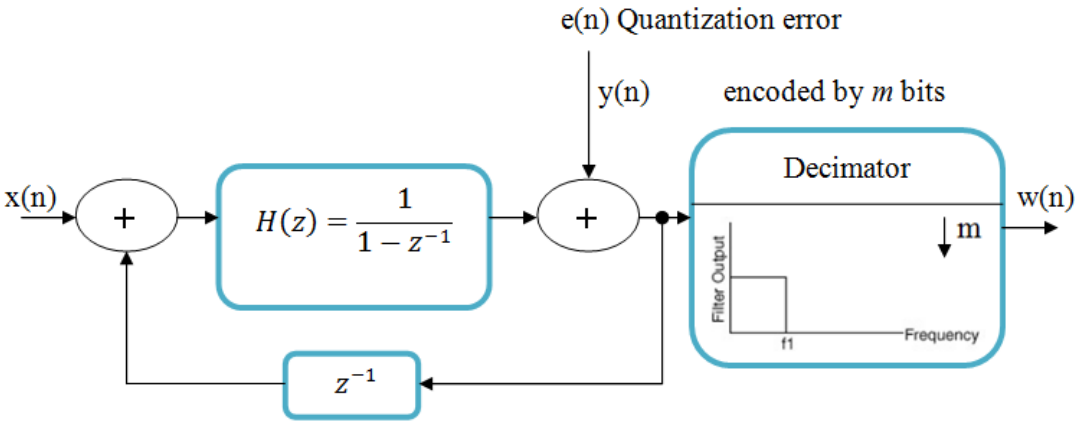

Figure.11 DSP model for the sigma delta modulator

By utilizing the z-transform and leads to,

$$Y(z) = (\ 1/1 - z^{-1}) + (X(z) - z^{-1}Y(z))\ + E(z) \quad (11)$$

The above equation represents,

$$Y(z) = X(z)\{Originaldigitalsignaltransform\} + (1 - z - 1) * highpassfilter + E(z)\{Quantization\ error\ transform\} \quad (12)$$

From the above equation, the high pass filter is used to induce the quantization noise whereas to maintain the maximum range of frequency value and then the noise quantization rate might be eliminated with the help of decimation filter. The decimation filter is the low pass filter. It has different architectural procedures and it has been used to execute the decimation filter. A comb filter that has a transfer function and the operation is described as,

$$H(z) = \left(\frac{1-z^{-ND}}{1-z^{-1}}\right)^{k} \quad (13)$$

Here, K is the filter order, N is considering as decimation factor and D represents the variation in delay. Figure 12, represents the non-recursive transfer function execution and the decimation filter resultant has been described by non-recursive architecture.

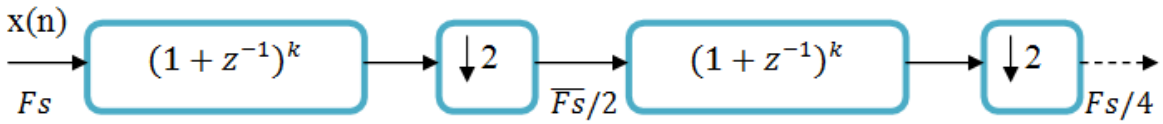

Figure.12 Non-recursive structure

2.2 Digital Comb Filter

"Comb Filters" are hair comb shaped filter with several "teeth", which are used as notches in the transfer function. These evenly distributed notches are used to remove the noise and it may appear at constant period of frequency. However, this comb filters have been utilized in a different collection of functions of signal processing. It can be like:

- Cascaded Integrator Comb channels, regularly utilized for against associating during interjection and demolition activity which may modify the example pace of a framework with discrete-time.
- There may be two different types of existence of Comb filters which is known as, Feed forward and Feedback. It refers to the orientation where the signal flow seems lagging in input when they are directly includes.

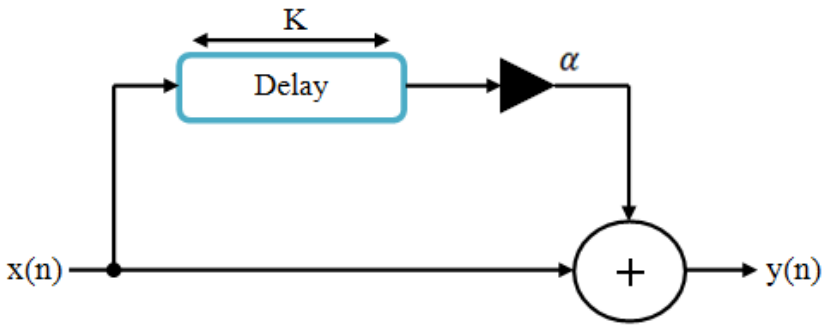

Figure.13 Feed forward comb filter structure

$$Y(n) = x(n) + \alpha\, x(n-k) \tag{14}$$

Let, k is the length lagging rate, and ∝ is referred as measuring terms involved to the lagged signals.

$$Y(z) = (1 + \alpha z^{-k})\, X(z) \tag{15}$$

We define the transfer function as:

$$H(z) = Y(z)/X(z) = 1 + \alpha z^{-k} = Z^k + \alpha/Z^k \tag{16}$$

Let us consider α as a positive value and the primary lower value occurs at partially and then the lagging and replicate time by its delay frequency and it may multiples,

$$f = 1/2K, 3/2K, 5/2K \tag{17}$$

2.3 Feed Backward Form

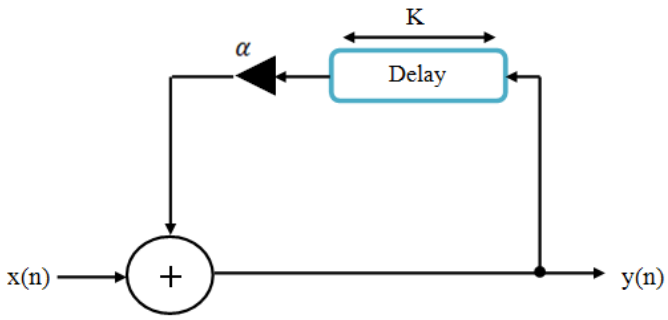

Figure.14 Feed backward comb filter structure

$$y(n) = x(n) + \alpha y(n-k) \tag{18}$$

Let us consider the Z transform and the outcome obtains:

$$(1 + \alpha z - k)Y(z) = X(z) \tag{19}$$

The transfer function is therefore

$$H(z) = Y(z)/X(z) = 1/(1 + \alpha z^{-k}) = Z^k/(Z^k - \alpha) \tag{20}$$

Let we imagineα as positive value and it may lower value takes place at 0 and it mat replicateby its delay frequency and it may multiples:

$$f = 0, 1/K, 2/K \tag{21}$$

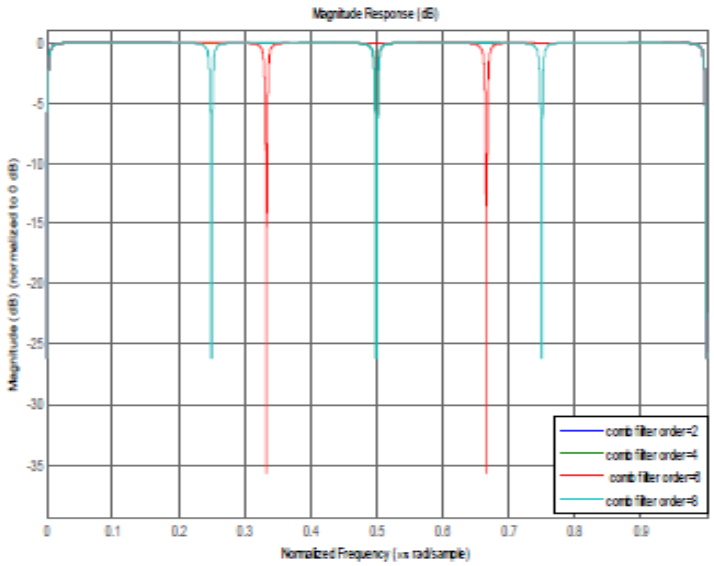

Figure.15 Comb filter Amplitude Frequency characteristics

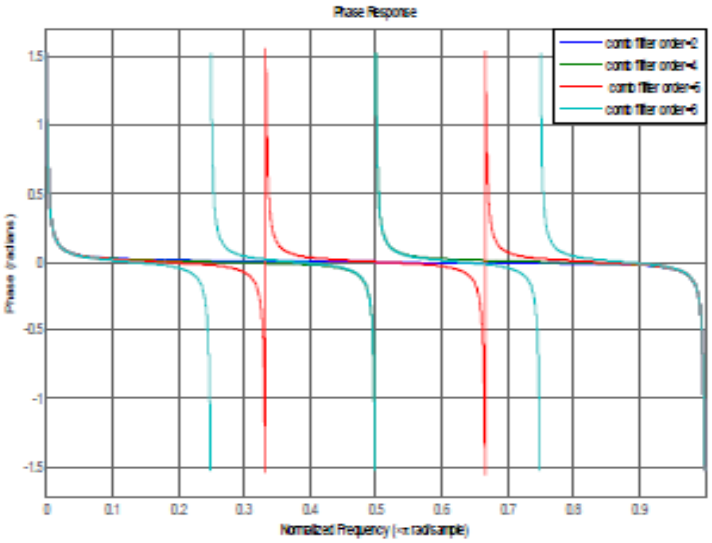

Figure.16 Comb filter phase response

2.4 Multilevel Stage Noise Shaping (MASH)

This proposed system architecture may refer as the fourth order MASH sigma delta modulator shown in Figure 17. However, the basic classic value is 2-1-1 MASH framework and the input and output difference of the prior step quantizer that is denoted by $\lambda_i$and $g_i$respectively, where as to utilize as next step input. As long as, this multiple bit ADC has been utilized and the

quantization noise is being quantized in the final stage. This process is known as ΣΔ ADC. Let we assume $\lambda_i = 1$, and finishing outcome has been achieved by means of get rid of the quantization noise for 2-1-1 MASH framework:

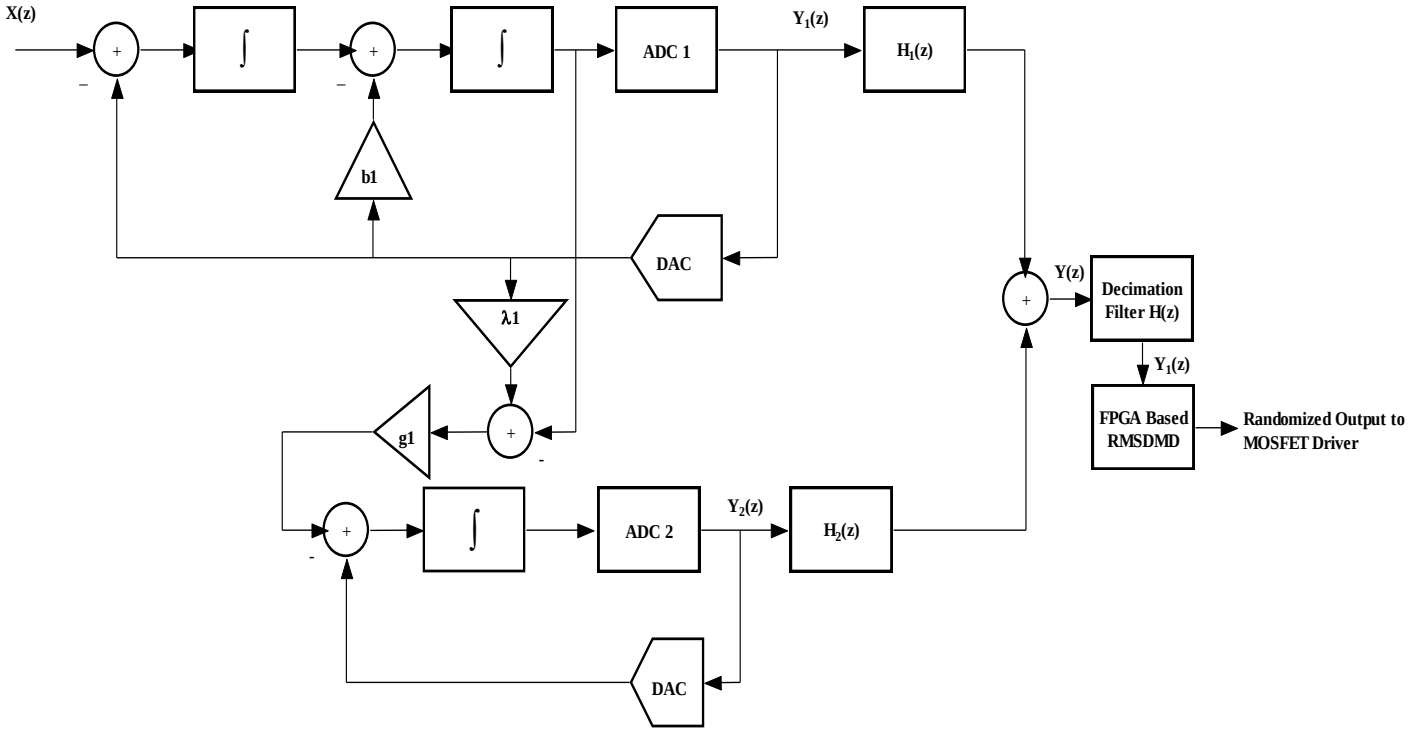

Figure.17 A Fourth order 2-1-1 MASH ΣΔ with decimator

The fourth order outcome of MASH ΣΔ modulator is shown below,

$$Y(z) = z^{-4}X(z) + \frac{1}{g_1 g_2 g_3}(1 - z^{-1})^4 Q_4(z) \tag{22}$$

Where $g_i$the inter-stage *is* gain and the quantization error is$Q4(z)$for the last step. The MASH quantization noise can be eliminated by using the comb filter can be used as a decimation filter. Whose output is given by,

$$Y_1(z) = Y(z).H(z) \tag{23}$$

Where,$H(z)$ is the transfer function of the Comb decimation filter. Therefore,

$$Y_1(z) = z^{-4}X(z) + \frac{1}{g1g2g3}(1 - z^{-1})^4 Q_4(z) \times H(z) \tag{24}$$

The above is the output of the 4thorder MASH ΣΔ modulator with a decimation filter. The MASH fourth order with multi-bit decimation filter ADC can offer a maximum degree value by means of concurrence and just about cost of linear hardware along with the declaration, however it may uncomplicated when comes to reconfiguration to a various declaration by accepting various steps. Hence, the decimation filter effectively removes all noise including high-

frequency quantization noise. By choosing the order of decimation comb filter improves the noise removal effectively, which can be modified by changing the value of N in the filter transfer function given below.

$$Y_1(z) = z^{-4}X(z) + \frac{1}{g1g2g3}(1 - z^{-1})^4\, Q_4(z) \times \left(\frac{1-z^{-ND}}{1-z^{-1}}\right)^k \tag{25}$$

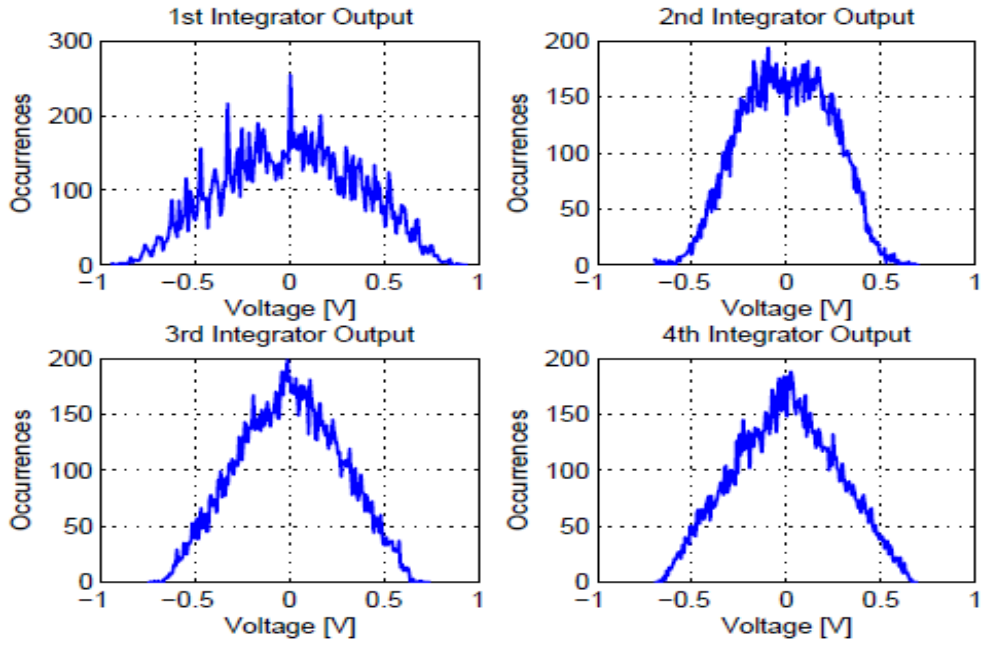

Figure.18 Histogram of each integrator outputs of the MASH sigma delta modulator

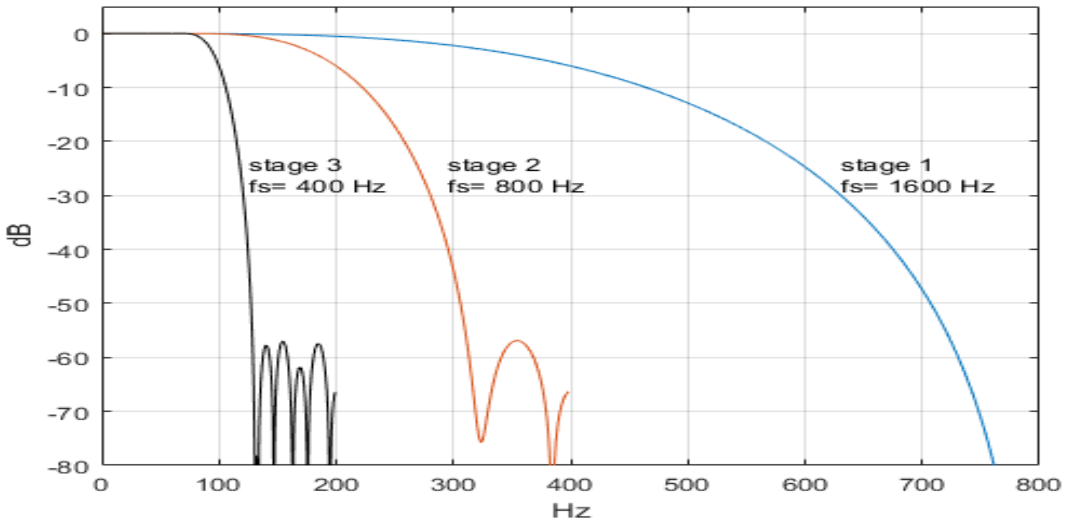

Figure.19 Output of Multistage Decimation Filter Response

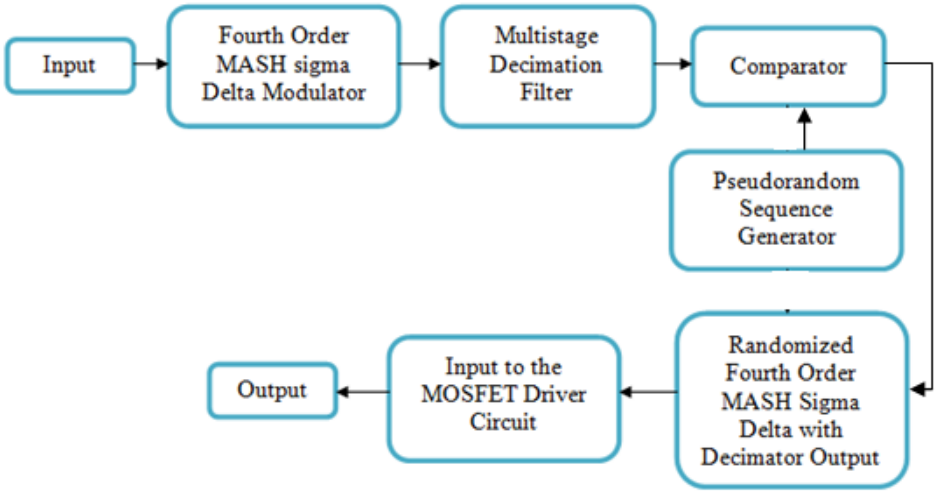

Figure.20 Multistage decimation filter

3. EXPERIMENTAL RESULTS AND DISCUSSION

The experimented setup for randomly switched multistage sigma-delta modulator with decimator filter for a DC to DC buck setup has been intended and executed by utilizing Altera based FPGA device EP4CE115F29C7 and Altera Quartus II synthesis software tool. The output inductor is structured by means a way so that continuous mode of conduction can be initiated by this converter. However, the common and differential mode noise current can be calculated by high-frequency current probe by the EMI receiver. This noise conduction can be calculated transversely whereas the line impedance stabilizing network as an input of the converter.

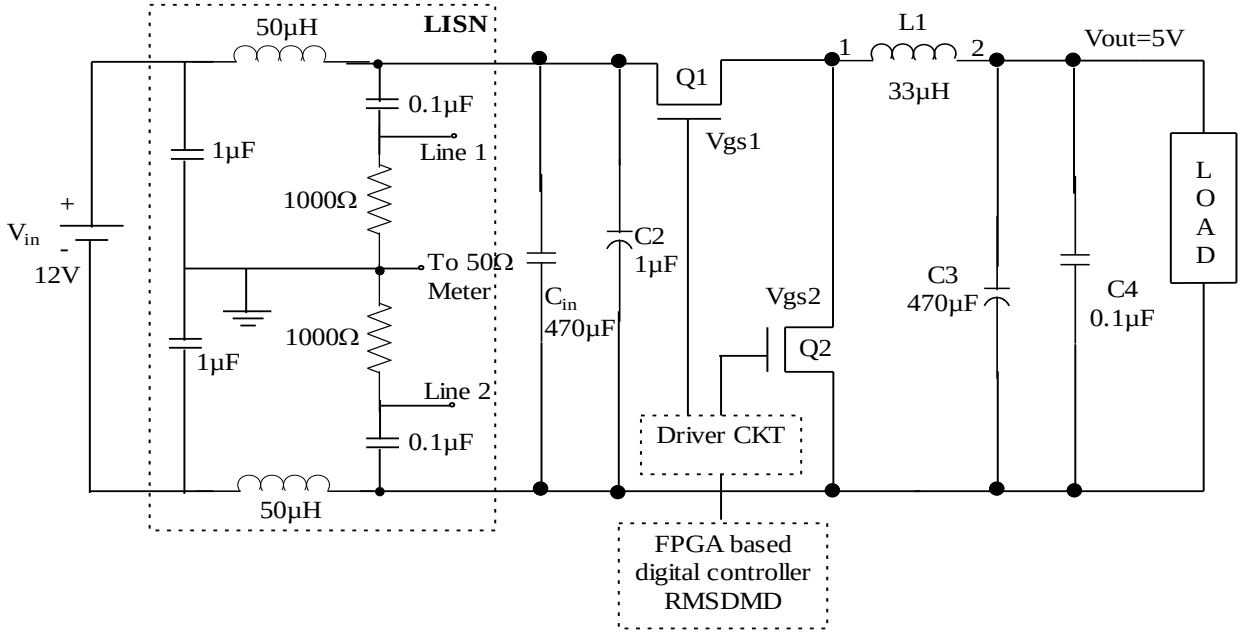

Figure.21 Conducted noise measurement circuit

The noise measurement is taken at Vin =12V, Vo=5V, and Po=100W, L Output inductor =33µH, C_o Output capacitor, C_{in} Input capacitor with a switching frequency 300khz, sampling frequency 400 Khz, and center duty ratio and resolution bandwidth of spectrum analyzer RBW = 40kHz. Figure 22, shows PSD (power spectrum density) of conventional PWM. Figure 23, shows PSD for RPWM compared with PWM. Figure 24, shows PSD compared with PWM and RMSDMD. The noise spectrum of the converter with DPWM is shown in Figure 25, and Figure 26, shows the conducted noise spectrum using randomized PWM. It's been identified from Figure 27, that the proposed RMSDMD digital controller shows significant improvement in the frequency spectrum of conducted noise that has been reduced according to FCC class B emission limit.

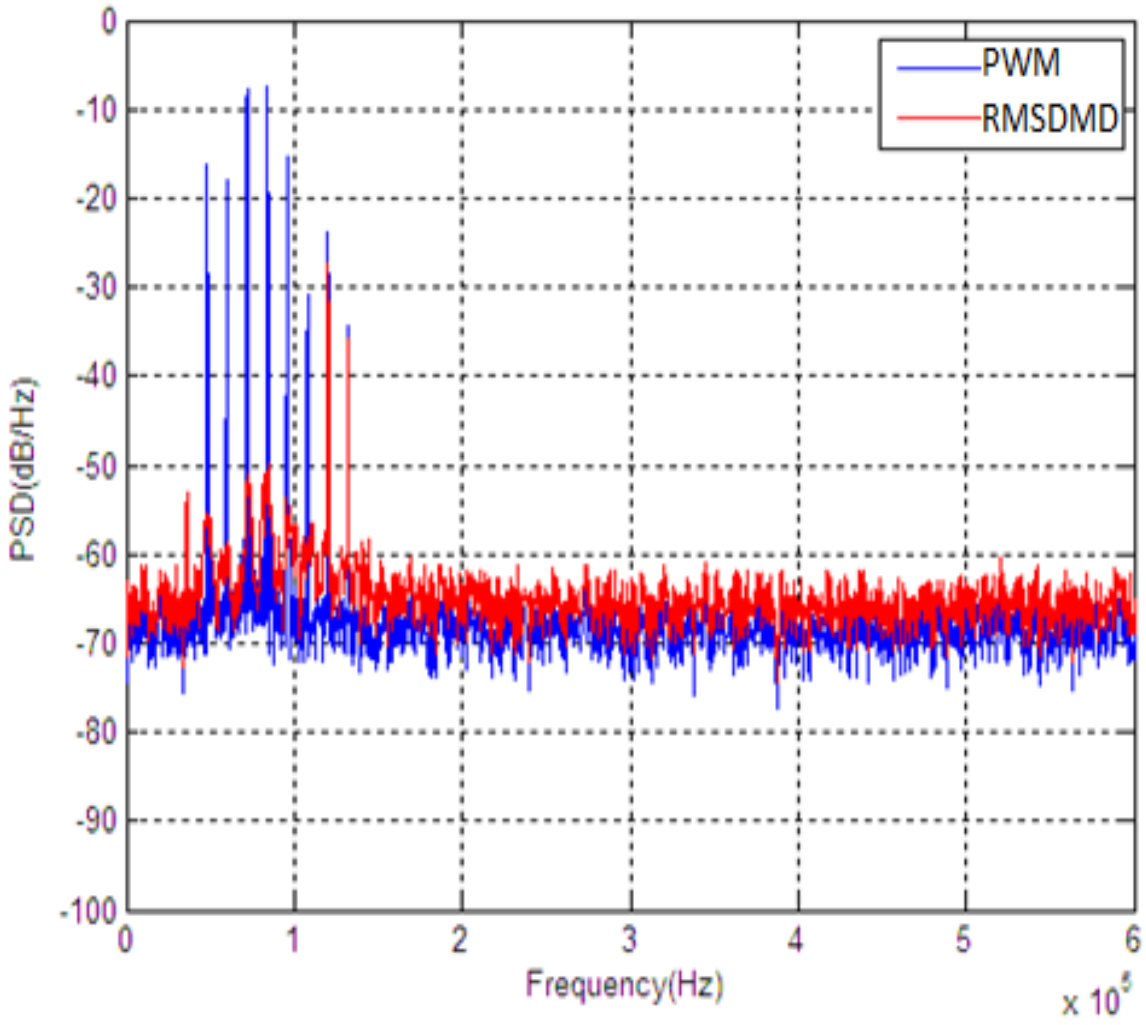

Figure.24 PSD output of RMSDMD

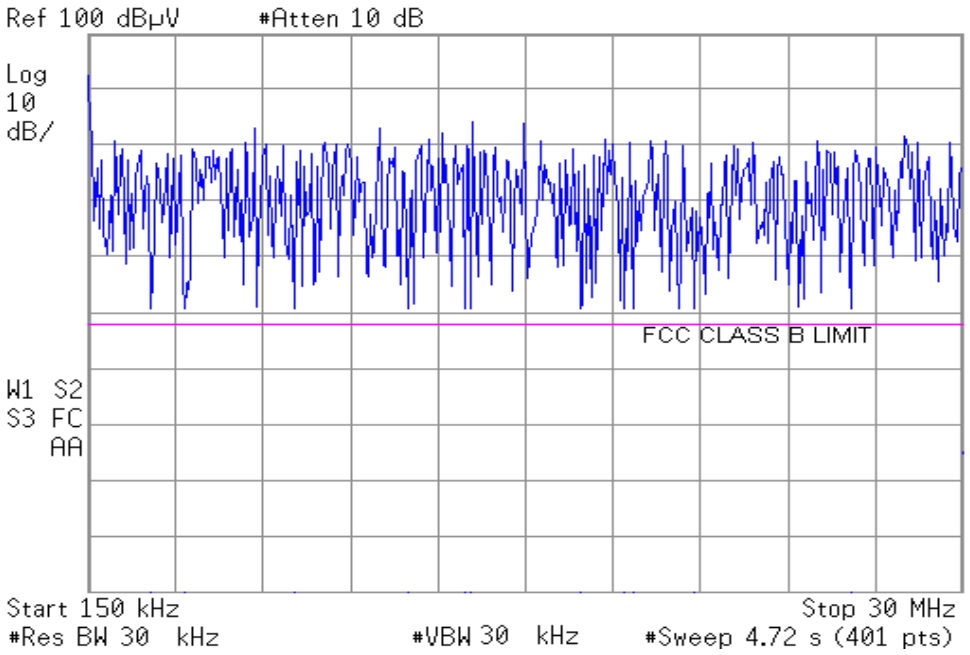

Figure.25 Conducted EMI of the PWM

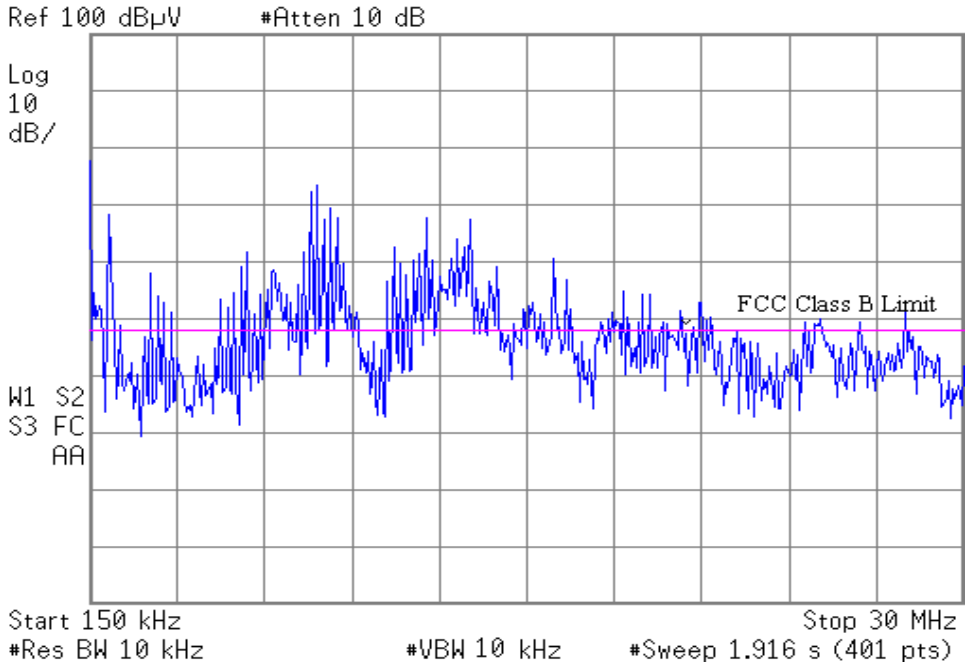

Figure.26 Conducted EMI of the RPWM

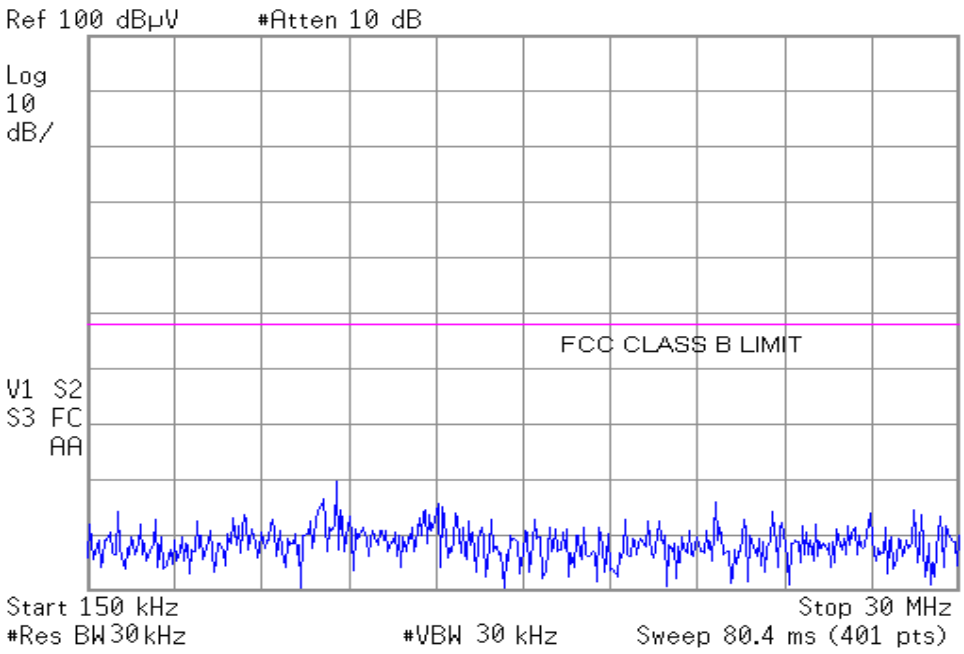

Figure.27 Conducted EMI of the proposed RMSDMD

Table.2 Comparison of PWM with RPPM and RMSDMD Schemes

Frequency in MHz	Conducted EMI results in $dB\mu V$		
	PWM	RPPM	RMSDMD
05	83	56	13
10	80	53	11
15	76	40	09

4. CONCLUSION

This article's main motive is to reduce the switching noise in the DC to DC converter and to implement the controller in an Altera FPGA device used to generate the PWM wave. A switching noise can be reduced by using spread spectrum method from higher spike to smooth and continuous spectrums as a result of applying randomization method in switch based converters then the noise conduction is reduced by its respective boundaries forced by the international FCC Class B principles. The experimental results have proven that the proposed randomized sigma-delta modulator with multi-stage decimator filter give better noise reduction compared to other PWM technique.

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