TRANSIMPEDANCE AMPLIFIER DESIGN FOR MILLISECOND CURRENT PULSES

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ABSTRACT. A 10^9 V/A gain, 5 kHz bandwidth transimpedance amplifier is designed and tested for noise limits close to the theoretical prediction. The amplifier is tested to amplify tiny current pulses coming out of Faraday cup detectors. Noise voltage referred to output (RTO) is measured and the input-referred current noise (RTI) is calculated and found to be 270 μV_{RMS} and 12.4 fA/$\sqrt{Hz}$ close to the theoretical limit of 246 μV_{RMS} and 10 fA/$\sqrt{Hz}$. We have concentrated on the amplifier topology, choice of op-amp, the feedback resistor and other components to optimize noise. Special attention has been given to the reduce the parasitic capacitance of the printed circuit board (PCB) and feedback resistor R_F package to further reduce and optimize the noise.

Keywords: Ion Mobility Spectrometer, Transimpedance amplifier, analytical instruments, amplifier noise, bandwidth.

I. INTRODUCTION

Millisecond duration current pulses are generated in variety of applications like radiation detectors [1], [2], chemiluminescence analyser [3], scanning tunnelling microscopy [4], [5], single-ion patch clamping, amperometric recording of single exocytotic events, detection of DNA molecules translocating through solid-state nanopores [6], Ion Mobility Spectrometer (IMS) [7], mass spectrometer [8] and in several other analytical instruments.

For example, the Faraday cup detector of IMS generates current pulses of several tens of picoamperes to about 100 picoamperes amplitude. To faithfully convert these current pulses into voltage, precision transimpedance amplifiers (TIAs) or current-to-voltage converters are used, for example [4]. The TIA requires 10^8 to 10^{11} V/A transimpedance gain and 5 kHz bandwidth at the lowest possible noise. In addition, the TIA sees a 30 pF source or detector capacitance from the Faraday cup detector contributing largely to the noise. The achievable theoretical input-referred current noise limit is 10 fA/$\sqrt{Hz}$ or output voltage noise for the given gain, bandwidth requirements, and source capacitance is 246 μV_{RMS}. Reducing the noise can decrease the amplitude of the smallest detectable current pulse at the amplifier input.

Many authors have tried to achieve the theoretical noise limit. But, the parasitic capacitances from the feedback resistor, printed circuit board (PCB), and cable make it difficult to achieve the theoretical noise limit. This article designed a 10^9 V/A transimpedance gain, 5 kHz bandwidth TIA with noise levels close to the theoretical limits. We have concentrated on several aspects from device selection, amplifier topology, guard ring, and running a trace under the feedback resistance to reduce

the feedback resistor parasitic capacitances. Noise performance of 270 μV$_{RMS}$ at the output or 12.4 fA/$\sqrt{Hz}$ input-referred current noises close to the theoretical limit of 246 μV$_{RMS}$ is achieved.

II. ION MOBILITY SPECTROMETER
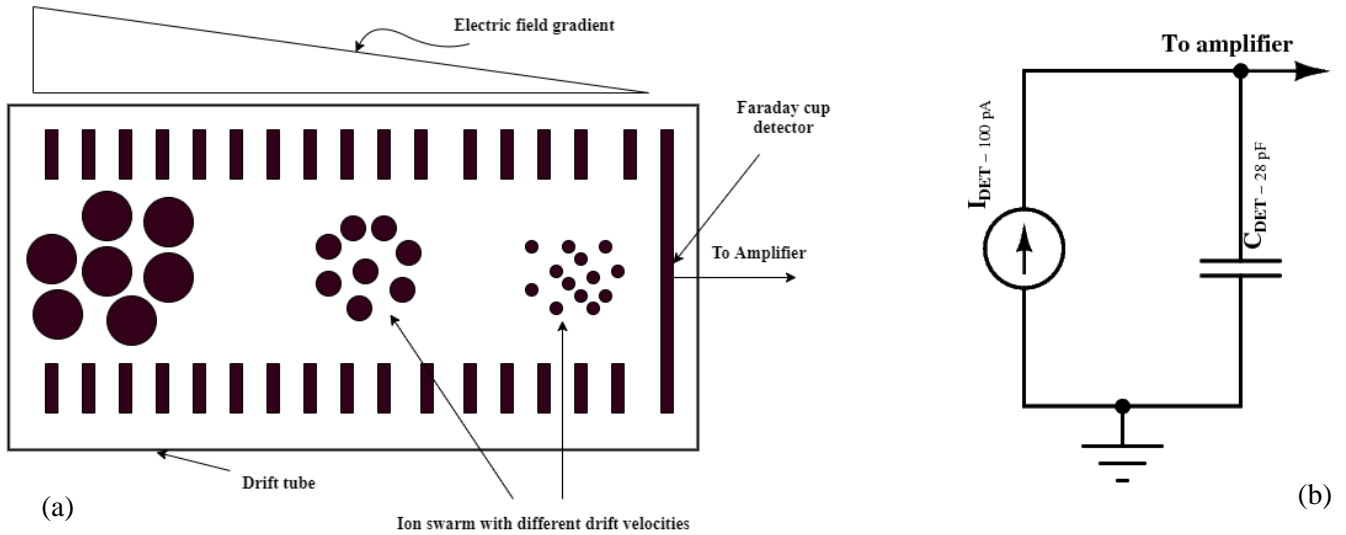
Figure 1. (a) Working principle of Ion Mobility Spectrometer IMS shown with Faraday detector   (b) equivalent circuit of the Faraday cup detector with source capacitance

IMS is an analytical technique used to identify chemical compounds present in the trace samples from their mobility information. Here, as shown in figure 1(a), the ions move in the presence of a high electric field and hit the detector. This process generates current pulses of 100 pA amplitude and 0.5 to 1 ms full width half maximum (FWHM) out of the detector.

The Faraday cup detector is modelled as a small current source and the detector capacitor can be modelled in parallel to the current source as shown in figure 1. The IMS that we tested our TIA uses the FC-72A Faraday cup from Kimball Physics, the USA with 28 pF source capacitance. The bandwidth requirement of the TIA to achieve the required FWHM can be calculated as
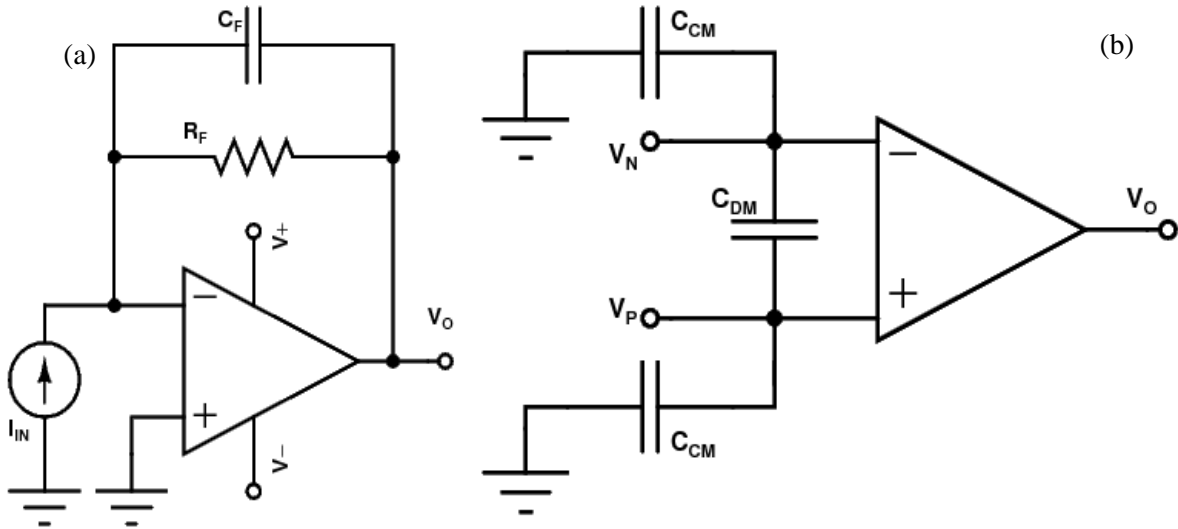
$$FWHM \times f_{-3\,dB} = 0.34$$

$$f_{-3\,dB} = \frac{0.35}{0.7\,m}$$

$$f_{-3dB} = 500\,Hz$$

The corresponding rise time (t_r) of the amplifier is $t_r = 0.7\,ms$. Though, in order to see even the sharp pulses, we choose 5 kHz bandwidth for our TIA.

III. LOW NOISE TRANSIMPEDANCE AMPLIFIER DESIGN PRINCIPLES

Figure 2(a) Basic TIA stage (b) operational amplifier non-idealities.

The basic TIA in figure 2(a) has an op-amp embedded in the negative feedback loop with the resistor R_F in the feedback path. Here, the feedback resistor R_F converts the input current into a voltage [9]. The value of the feedback resistor is the transimpedance gain of the amplifier.

$$V_0 = -R_F I_{IN}$$

As shown in figure 2 (b), the op-amp has common-mode (C_{CM}) and differential mode (C_{DM}) capacitance at its input terminals. This capacitance along with the detector source capacitance leads to potential stability issues. To compensate for the input capacitance and to ensure stability, [10], [11], [12] a small feedback capacitor parallel to R_F is used. The feedback resistor R_F along with the feedback capacitor C_F determines the bandwidth of the TIA. Also, choosing the gain and the bandwidth gives the value of the feedback capacitance.

$$f_{-3dB} = \frac{1}{2\pi R_F C_F}$$

For maximally-flat, second order and Butterworth frequency response the values of RF and CF should comply the following equation

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_F}}$$

For large input capacitance, an op-amp with higher gain-bandwidth product (GBP) is desired to avoid failure related to stability [4], [14]. A large GBP and large transimpedance gain lead to very small values in the femto Farads for the feedback capacitor C_F. Realizing capacitors less than 0.1 pF are very difficult. This is one of the biggest challenges in high gain, low noise TIAs. The TIA input-referred current noise is given by the following equation

$$i_{EQ} = \sqrt{i_N{}^2 + \frac{4kT}{R_F} + \left(\frac{e_N}{R_F}\right)^2 + \frac{(e_N 2\pi C_{TOT}f)^2}{3}}$$

Alternatively, the output noise voltage can be given as

$$V_{OUTN} = \sqrt{(I_N R_F)^2 + 4kTR_F + e_N{}^2 + \frac{(e_N 2\pi C_{TOT}R_F F)^2}{3}}$$

The first and third terms represent noise due to the op-amp current and voltage noise densities. These two terms are of negligible magnitude. The second term represents the noise contribution of the feedback resistor and one of the major noise sources. A large resistor produces large noise. The fourth term in the equation is another major source of the noise. This noise arises due to the op-amp noise voltage source, e_N, appearing in parallel to the various capacitances lumped as C_{TOT}. Where C_{TOT} is given by

$$C_{TOT} = C_{DET} + C_{CM} + C_{DM} + C_{par}$$

C_{TOT} is the sum of detector or source capacitance (C_{DET}), op-amp common-mode (C_{CM}) and differential- mode (C_{DM}) capacitances, and C_{par} which is the parasitic capacitance of the feedback resistor, PCB board parasitic capacitance, and any other parasitic capacitances contribute to the C_{TOT}. Reducing C_{TOT} will improve the noise performance. Among these capacitances, C_{CM} and C_{DM} can be reduced by choosing low capacitance op-amps. C_{par} can be reduced by proper layout techniques.

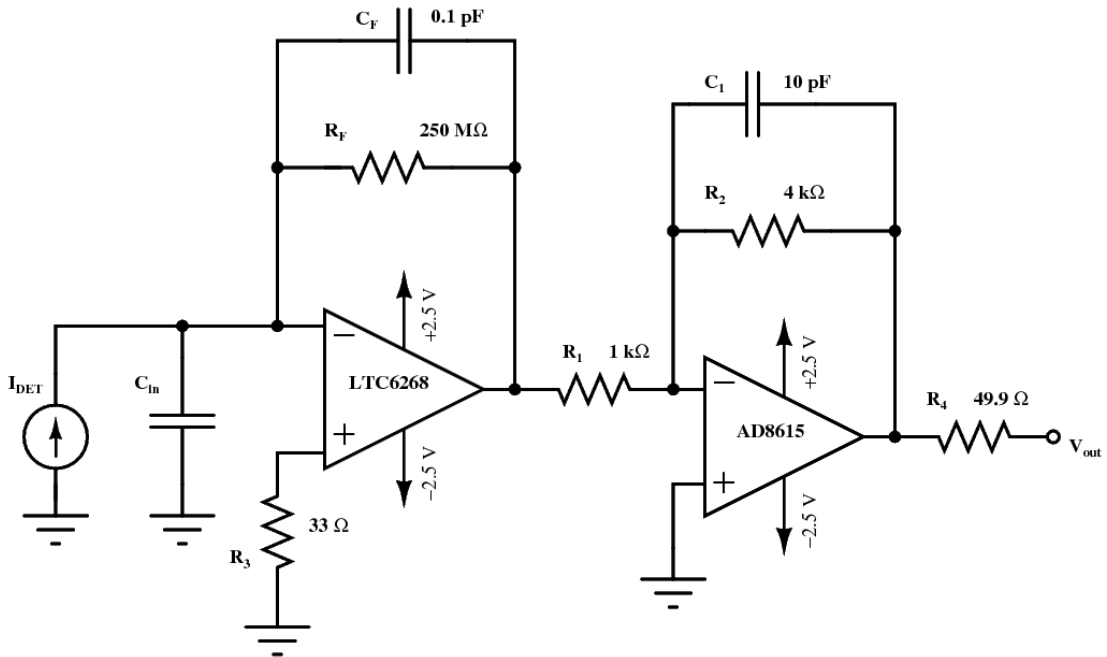## IV. TRANSIMPEDANCE AMPLIFIER DESIGN, FABRICATION AND CHOICE OF COMPONENTS

Figure 3. Low noise, two-stage transimpedance amplifier

Figure 3 shows the TIA that we have designed. We have chosen the two-stage [15] design to reduce the value of R_F. A large resistor has large parasitic capacitance across it and increases the noise. The first stage is the transimpedance stage with 250 x 10^6 V/A gain and the second one is the inverting amplifier with a gain of 4 V/V. The overall transimpedance gain is 10^9 V/A. The feedback capacitor in the first stage is set to 0.1 pF so that the 3-dB bandwidth of the circuit is 5 kHz.

Also, much of the gain is reserved for the first transimpedance stage. The noise contribution from the second amplifier stage is lesser when compared to the first stage amplifier. A 10 pF capacitor is added in parallel to the resistor R_2 to roll-off the high frequency gain in the second stage and reduce subsequent noise.

Special attention is given to choose the op-amp for the design. Particularly, the first stage operational amplifier is the critical element in the TIA design. The op-amp chosen is expected to have large GBP [13], [10], lowest possible input capacitance [4], input bias current and voltage and current densities [26]. Several op-amps were shortlisted for the first stage as listed in the Table 1.

Table 1 Comparison of operational amplifiers and their parameters suitable for TIA

OP-AMP	GBWP (MHz)	I_b (pA)	C_{in} (pF) (C_{CM} + C_{DM})	e_n ($nV/\sqrt{Hz}$)	i_n ($fA/\sqrt{Hz}$)
LTC6268	500	0.003	0.45	4.3	5.5
OPA656	230	2	3.5	7	1.3
LMH6629	900	2	5.7	0.69	2600
OPA657	1600	2	3.5	4.8	1.3
LMC662	1.4	0.002	< 10	22	0.2
LMP7721	88	0.1	< 10	5.8	0.01
ADA4530-1	2	0.02	8	14	0.07

Amongst the op-amps listed in Table 1, OPA657 [16] and OPA656 [17] offer better GBP, voltage and current noise densities. But, their capacitance is large when compared to the LTC6268 [18]. Next, LMH6629 [19] has better voltage noise and good bandwidth but the current noise and bias currents are large compared to LTC6268. LMC662 [20] offers low bias current, lower voltage and current densities but the GBP is less. Likewise the capacitance of LMP7721 [21] is larger than LTC6268. ADA4530-1 [22] offers low bias currents and current noise. But, the voltage is very high, GBP is lesser and input capacitance is much larger than LTC6268.

In addition to comparing these parameters, the best op-amp for low noise can be compared from CV + I noise comparison of these op-amps. The CV + I noise is useful method to compare noise performance of different op-amps. It is given by

$$I_{NOISE,CV + I} = \sqrt{(2\pi f C_{IN} e_N)^2 + (i_N)^2}$$

Because of negative feedback, the inverting input is sitting at virtual ground. Therefore, i_N pass through R_F with gain of 1 and it can be neglected. Now, the CV + I noise becomes

$$I_{NOISE,CV+I} = 2\pi f C_{IN} e_N$$

Comparing the CV + I noise for various op-amps will give a quantified idea of which op-amp can be used for the design. The CV + I noise of various op-amps is given in Table. The CV + I noise of LTC6268 is the lowest of all the op-amps listed.

Table 2. CV + I noise comparison of different operational amplifiers

OP-AMP	CV + I Noise (@ 5 kHz) $fA/\sqrt{Hz}$
LTC6268	0.07
OPA656	0.7
LMH6629	2600
OPA657	0.5
LMC662	7
LMP7721	1.8
ADA4530-1	3.5

Based on the above discussion, LTC6268 is the best op-amp for our application. It offers larger GBP, lower bias currents, lower voltage and current densities. The most important feature of LTC6268 is that its lowest possible input capacitances. Its C_{CM} is 0.45 pF and C_{DM} is 0.1 pF adding up to 0.55 pF input capacitance. Moreover, the LTC6268 allows technique to route the ground trace below the R_F to reduce its parasitic capacitance. In addition to that, the lower bias current reduces the error and disturbance in the system. Furthermore, the addition of guard ring in the layout reduces the disturbance to the input and reduces the noise further. Because of these features, the parasitic capacitance of the R_F is very less and in fact no compensation feedback capacitance is needed. This also drastically increases the bandwidth of the TIA. Though, a 0.1 pF feedback capacitor is added to restrict the bandwidth to about 5 kHz

For the second stage, AD8615, a rail-to-rail-output (RRIO) from Analog Devices is used in the design. It is a 24 MHz GBP, $7\ nV/\sqrt{Hz}$ and $0.05\ pA/\sqrt{Hz}$ voltage and current noise densities are used. The circuit uses HVC1206Z2506JET high voltage, 5% tolerance, and 1206 pad size chip thick film resistors for the feedback resistor [24]. We used low temperature drift NP0/C0G capacitors for the feedback capacitor.

The circuit is powered with ±2.5 V DC power supply. To reduce the noise we used linear power supplies from low dropout regulators (LDO's). ADP7118ARDZ-2.5-R7, 200 mA positive voltage regulator [25] and ADP7182ARDZ-2.5-R7, 200 mA negative voltage regulators [26] from Analog Devices Inc., USA supplies the positive and negative voltages. 0.1 µF capacitors are used as power supply bypass capacitors.

The circuit is housed in a double-sided PCB made from FR4 material. The amplifier is housed in a 2 mm, IP54 rated thick die-cast ingress-protection aluminium box. A 2451 BNC female receptacle [26] from Pomona Electronics, USA connects the input to the amplifier board. This is a 50 Ω impedance gold plated beryllium copper centre contacts with tarnish resistant plating and PTFE dielectric suitable for low current applications. Output is taken to digital storage oscilloscope (DSO)

with 031-203-RFX 50 Ω BNC receptacle [27] from Amphenol. The detector current enters the amplifier via 115101-05-06.00 coaxial cable from Amphenol.

V. CIRCUIT SIMULATION

The TIA circuit is simulated LTSpice XVII software from Analog Devices for time response, frequency response and RMS output noise voltage. The input-referred noise is calculated from this RMS noise voltage. A 100 pA peak Gaussian signal is generated for testing the amplifier time response. The simulated response can be seen in Figure 4. The peak output voltage is 100 mV confirming the gain.
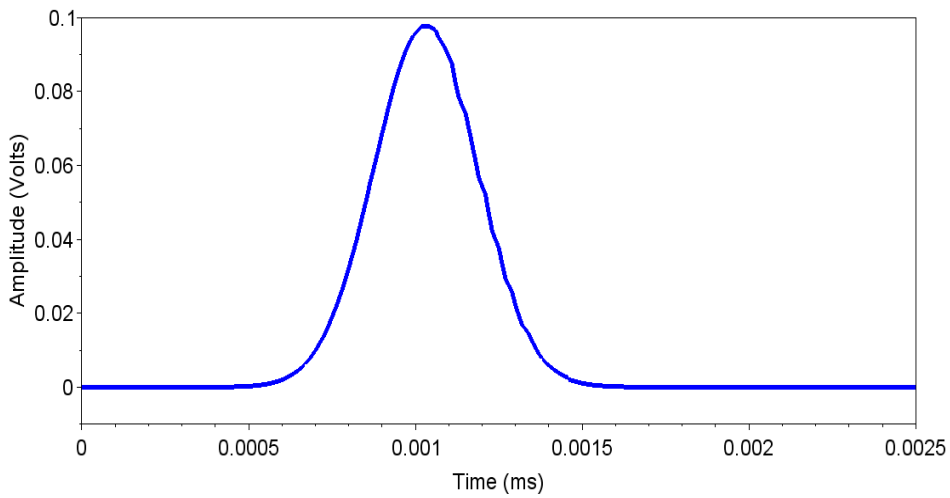

Figure 4. Transient response simulation of the low noise, two-stage TIA

The simulated frequency response of the amplifier is seen in Figure 5 where the amplitude o the test input signal is swept from 1 Hz to 1 MHz. Similarly, the RMS output noise of the signal is found in the figure 6. The simulated output shows the RMS voltage at the output as 246 μV$_{RMS}$.
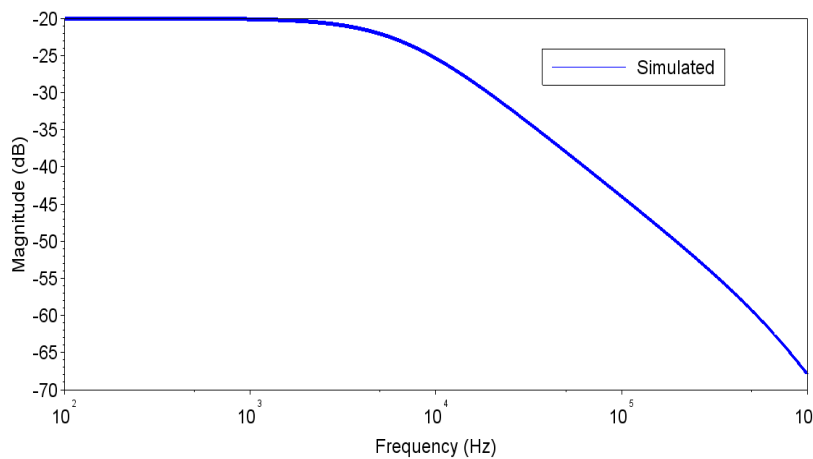
Figure 5. Frequency response simulation of the low noise, two-stage TIA
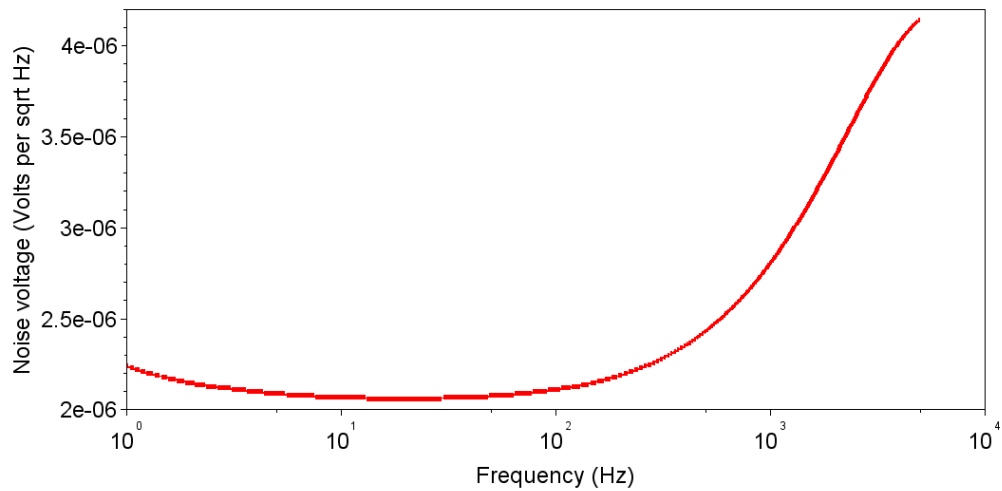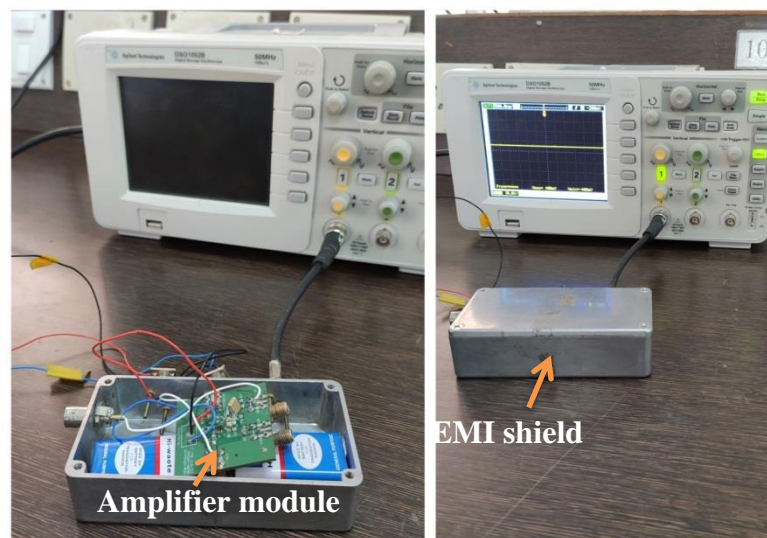
Figure 6. Simulated noise voltage density of the low noise, two-stage TIA

VI. EXPERIMENTAL SETUP AND RESULTS

i. Experimental Setup:

An aluminium metal box houses the amplifier to prevent the circuit from external electromagnetic interference (EMI). The circuit is connected to the DSO with on-board SMA connectors and via the BNC connector.


Figure 7. Experimental set up

ii. DC Transfer characteristics:

To measure the DC transfer characteristics of the circuit, a small voltage is generated with a potential divider of voltage ratio 100: 1. The generated voltage is then buffered with precision op-amp. Then, a high value 1% precision resistor converts this small voltage into a small current around 100 pA. Currents up to 200 pA was generated. These currents are then used to test the DC performance

characteristics of the TIA. The simulated and measured DC transfer characteristics were plotted in figure 8.
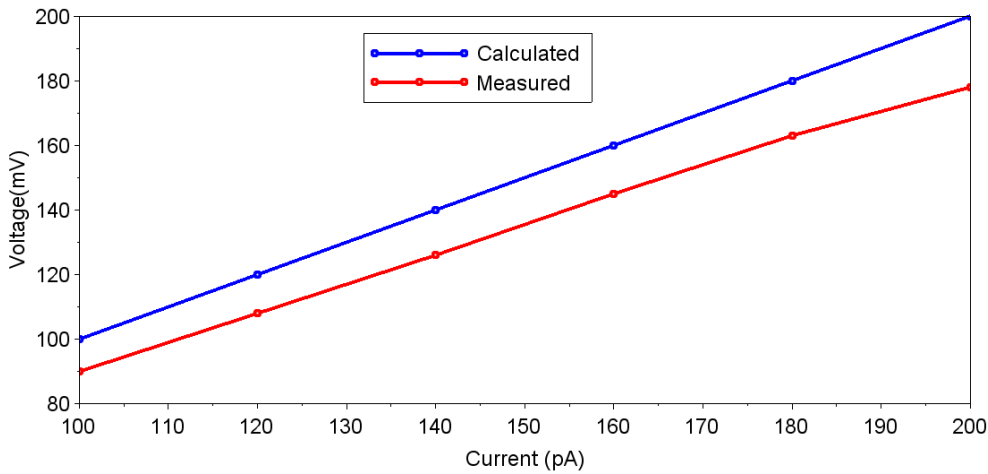
Figure 8. Measured DC transfer characteristic of the TIA

iii. AC Transfer characteristics Measurement:

Sine wave signals of different frequencies are generated using AD9833 [28] Direct Digital Synthesis (DDS) IC and attenuated with precision opamp circuits. They are then filtered and passed through a small NP0 capacitor to generate sinusoidal currents with 100 pA amplitude [10]. A 100 pA peak-to-peak sinusoidal test signal measures the frequency response between 10 Hz and 1 MHz frequency range. The measured response is plotted in figure 9.

The amplifier is designed for 10^9 V/A transimpedance gain. Because of the parasitic capacitance of the feedback resistor we are unable to meet the theoretical gain. Measurement results show that a nominal gain of 0.9 x 10^9 V/A is always achieved.
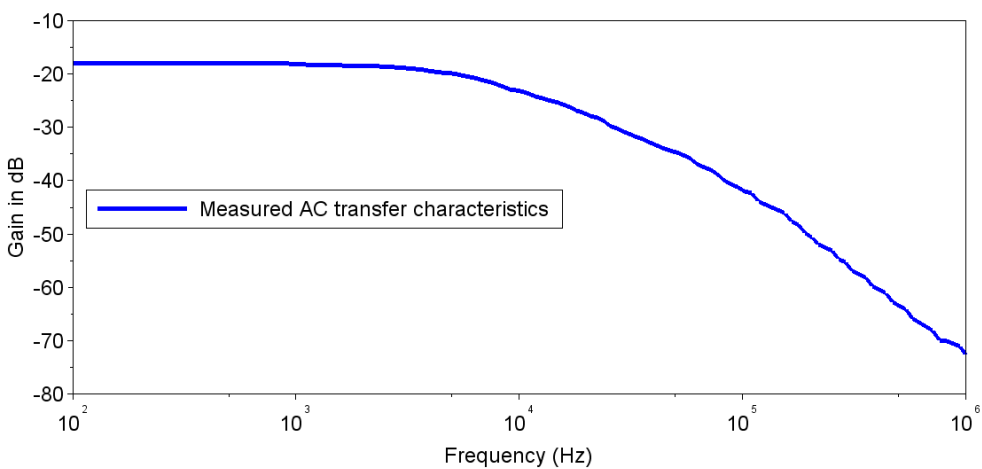

Figure 9. Measured frequency response of the low noise, two-stage TIA

The amplifier is tested with a real Faraday cup detector FC-72A [29] from Kimball Physics, USA. The measured signals for water vapour are shown in figure 10. Waveform A is the averaged waveform and waveform B is the original waveform. The amplitude of the waveform is about 90 mV which confirms the theoretical prediction.
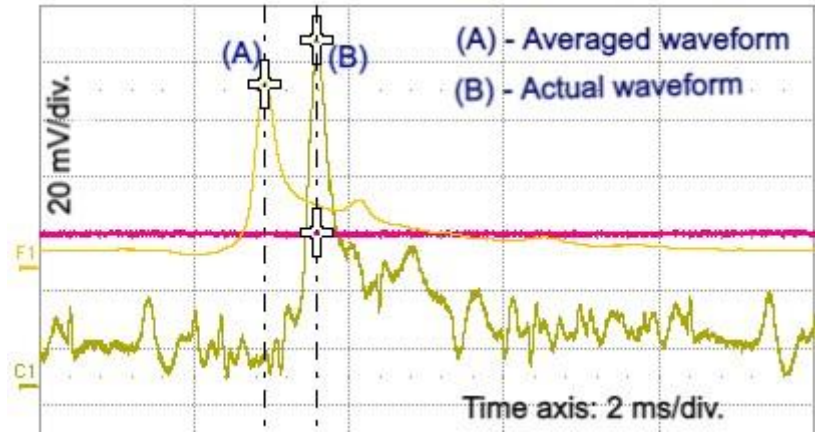
Figure 10. Measurement results of the fabricated amplifier is tested with a real Faraday cup detector

VII. NOISE MEASUREMENT
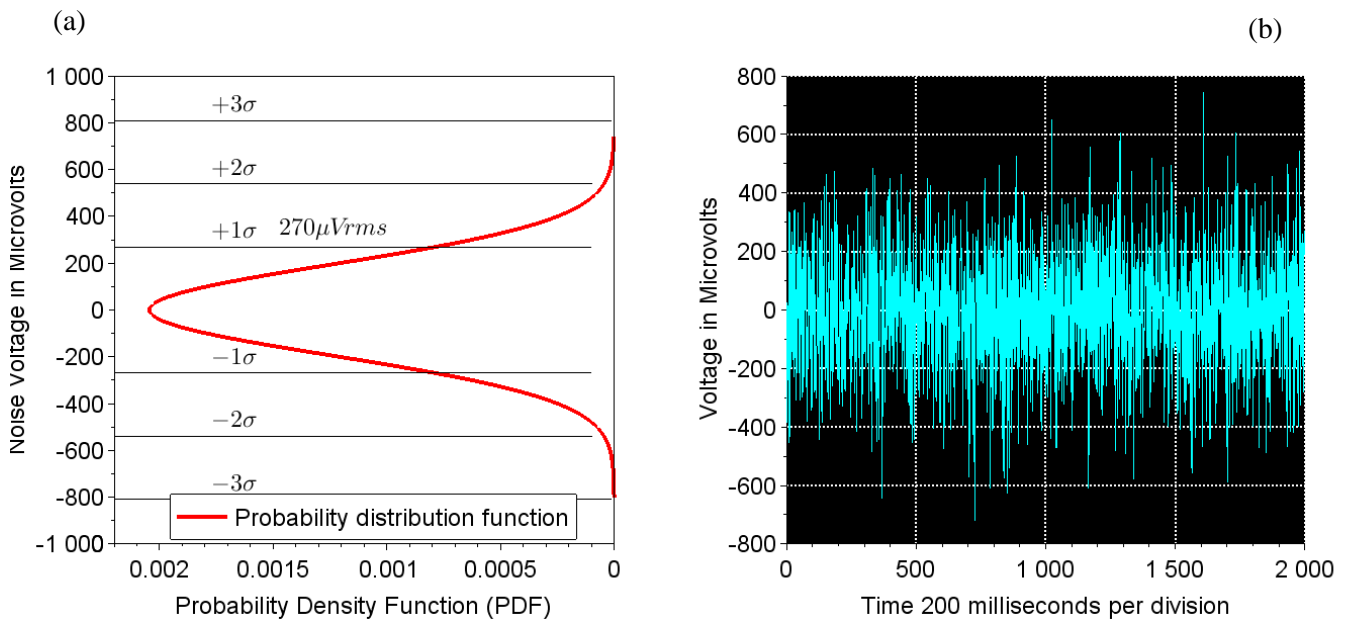
Figure 11. Measured noise signal (a) probability density function of the measured noise signal with RMS noise voltage and noise distribution (b) noise signal as viewed with a DSO

The RMS noise is measured with DSO. The RMS is found to be 270 μV_{RMS}. Statistically, it is the standard deviation and is equal to the RMS voltage. Figure 11 (b) shows the DSO waveform of the noise signal and figure 10(a) shows the Gaussian distribution of noise signal. It can be seen that the maximum of the noise distribution lies within the 2σ within two times of the standard deviation. Also evident is that about 99.7 % noise signal falls within 6σ. The measured noise is 270 μV_{RMS} which is close to the theoretical limit of 246 μV_{RMS}. The measured RMS voltage noise corresponds to

$12.4\ fA/\sqrt{Hz}$ input-referred noise at 30 pF input capacitance and 5 kHz system bandwidth. We have achieved noise performance close to the theoretical limit at this high capacitance. The noise floor is $12.4\ fA/\sqrt{Hz}$ and it is clear that the TIA is capable of amplifying even a minuscule of signal.

VIII. DISCUSSION

i. Guard ring
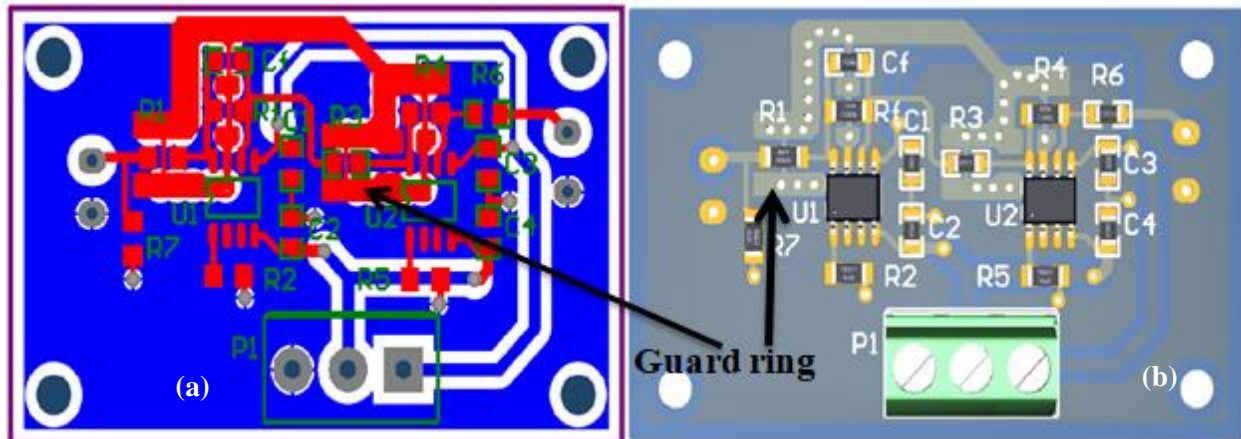
Figure 12. PCB layout of the TIA along with the guard rings.

As mentioned, the TIA that we have designed has input referred noise of $12.4\ fA/\sqrt{Hz}$ and output voltage noise is $270\ \mu V_{RMS}$ and is close to the theoretical limit of $246\ \mu V_{RMS}$. This was achieved by careful PCB layout and with other low-noise techniques. First of all, care was taken to reduce the parasitic capacitance. Choosing LTC6268 reduces the op-amp input capacitance contribution at just 0.55 pF. The next major source of parasitic capacitance is the feedback resistor. We have chosen 1206 sized surface mount technology precision resistor. The electric field E between the resistor pads is the source of the parasitic capacitance. A ground trace is run just under the trace of the feedback resistor R_F. This shields the electric field from one pad reaching the other pad and thus effectively reducing the parasitic capacitance.

In addition to this, the input bias current of LTC6268 is just 3 fA. But, leakage current from adjacent signal layers, board contamination, PCB material could increase it. This could introduce disturbance to the input signals. To decrease the effect of this, as shown in figure 10, a guard ring was laid out protecting the input path between the input connector and the inverting input of the op-amp. It is a copper-filled shape that completely surrounds the high impedance trace. The guard-ring creates a low-impedance path to the ground plane and absorbs any leakage or disturbance currents to the ground. The low input bias current combined with the guard ring reduces the disturbance to the input signal. This reduces the noise and the error contribution due to input bias current.

Moreover, the feedback resistor is placed as close as possible to the op-amp inverting pin. All the traces are kept as short as possible. We chose SOIC op-amp package. This package isolates the input pins from other signals on the four sides of the package. The gull-wing leads on SOIC package allow better cleaning of the PCB and reduced contamination-induced leakage. High impedance node is susceptible to picking up stray signals. Hence, the entire high impedance signal

path from the input BNC to the non-inverting pin is kept short. Keeping it as short as possible reduces this effect. Since this is a high impedance input node; no signals routed close to this signal path. Also, there is no power planes routed under this pin. Slotting the guard ring tracks provide additional isolation and reduce the effects of contamination. Solder flux, body oils, dust and dirt are all sources of contamination and can increase leakage currents along the high impedance traces. In addition to this, humidity will increase the leakage current. Therefore, the PCB is cleared with isopropyl alcohol (IPA). Also, the PCB is allowed to evaporate the residual moisture completely. This evaporation process took hours since we did not bake the PCB with an oven.

The TIA designed is compared with two other works [4] and [13]. [4] reported a noise performance of about 10^9 V/A transimpedance gain AND 100×10^{-13} A input referred noise at 1 nF capacitance and 4 kHz bandwidth designed with the op-amp OPA404. Likewise, [13] has designed an amplifier with 100 MΩ gain, 500 kHz bandwidth with 7.4 mV$_{RMS}$ noise voltage use LTC6268-10, a 4 GHz GBP version of LTC6268. Since, both amplifiers are designed for different set of parameters direct comparison is not possible and they are compared with linear scaling of parameters. When compared for input-referred noise, [4] reports about $300\ fA/\sqrt{Hz}$ and similarly for [13], the input-referred noise is about $14\ fA/\sqrt{Hz}$ which is just 1% more noise than our amplifier.

IX. CONCLUSION

We have designed, fabricated and tested a TIA with 10^9 V/A transimpedance gain and 5 kHz bandwidth at $12.4\ fA/\sqrt{Hz}$ input-referred noise (RTI) and 270 µV$_{RMS}$ output voltage noise (RTO). The results are compared with [4] and [13] and found to be better than them. By carefully concentrating on the choice of the main op-amp, PCB layout, using a guard ring, and running ground trace under the feedback resistor we reduced the parasitic capacitance of the board. We have optimized the noise close to its theoretical limits. Though, because it is not possible to eliminate the parasitic capacitances completely and because of unknown effects, we are not able to achieve the exact theoretical limits. But, we have achieved results closer to the theoretical limits.

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