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DESIGN OF ADDER BASED ON LOGICAL GATES FOR HIGHSPEED LOW POWER ROBOTIC APPLICATIONS

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Abstract. The low power analog and digital systems are the major for any robotic applications. Designing low power and high-speed digital systems is one of the major and essential needs in VLSI Systems. Adder is the main key block in the digital systems. The entire digital systems performance is based on this adder block, which decides the overall power consumption and speed of the circuit. Various early designed full adder cell circuits encountered with low speed and high-power consumption issues. Here novel 1-bit full adder is designed based on XOR and XNOR Cell structure which operates in full swing and also the no critical path. With the use of three proposed modules the sum and carry is obtained. The main objective of this proposed full adder is to bring minimum power consumption and delay. The novel proposed full adder provides less power consumption by 94.68%, 90.82%, 84.54%, 35.61% and 83.43% while comparing with other full compared adders. The simulations were obtained in DSCH and Microwind tool.

Keywords: Full Adder design, XOR gate, XNOR gate, High speed, Robotics, Low power.

1.Introduction

In recent years, most of the devices are designed based on the digital logic. The digital logic contains only two logics. Logic 0 and Logic 1. These two numbers dominates the whole world with new technology innovation and computer design. CMOS technology is one of the important principles for mixed signal integrated circuits especially for the communication systems. For the need of high speed communication devices clock speed and transistor size become vital part. In recent days millions of transistors are working at gigahertz.

Due to development of Nano technology in VLSI (very large scale integration) the design of more and more complex circuits are possible. Also the demand in digital technology, designing an efficient circuit is very much needed for design engineers. The digital circuits dominate in microelectronics applications like Mobile systems, Communication Systems, Sensor Networks, Internet of Things Applications etc., These requirements impose the low power and high speed logic circuits. In Digital Signal processors and many VLSI architectures uses the general arithmetic operations like addition, subtraction, multiplication in hardly.Since from several years, Full adder is a main focal element in the arithmetic blocks. For implementingthis arithmetic operation the full adder block is very essential. The entire arithmetic circuit's performance is depends mainly on adder circuit performance. CMOS (Complementary metal oxide silicon) technology has some greater characteristics like less fabrication cost, consumes less power consumption and ease implementation. Hence the CMOS is the dominant technology for integrated circuit design. Both digital andanalog circuits can be placed during the fabrication. This tends to reduce the fabrication cost as very low. As mentioned the power consumption of a digital circuits due to changes between the two logic values, the typical power consumption is less in CMOS technology.

The overall power dissipated in complementary metal oxide semiconductordesign is given as

$$P_{Total} = CV_{DD}^2 f + I_{sc}V_{DD} + I_{Leak}V_{DD} \quad (1)$$

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$$P_{Total} = P_{Dynamic} + P_{Short\ Circuit} + P_{Static} \quad (2)$$

During fabrication the area of the silicon decides the power consumption. The selection of logic style of any circuit will decides the efficiency of physical design. Placing the transistor and routing in physical design is mainly considered for reducing power and delay of the design. Based on this view, CMOS based styles of full adders are considered for this work.

The basic fundamental operation of any digital circuit is addition. So the efforts are made for getting efficient adder design or structures. A full adder circuit has three inputs and two outputs. The outputs are addition of three inputs. The inputs are A, B and C_{in}. The C_{in} input is derived from previous block or adder cell. The outputs of these three inputs are sum and C_{out} (Carry). The equations of single bit full adder is

$$Sum = A \oplus B \oplus C \quad (3)$$

$$Cout = A.B + B.Cin + Cin.A \quad (4)$$

The optimization states that method to get maximum or minimum output with minimal adjustments of mathematical equation and suitable design. By reducing the W/L ratio the circuit Power Delay Product is decreased instead of reducing the power supply voltage.

The most general conventional style has pull up and pull down structure. The PMOS transistor is connected in series and parallel manner in pull-up network. Similarly NMOS transistor is connected in series and parallel form in pull-down. This complex conventional style of design consumes more power than hybrid style. The main reason for the large power consumption is due to switching activity and short circuit current. Similarly capacitance effect in conventional method causes reduction in speed of operation.

Therefore a new XOR XNOR based full adder is proposed in this paper to attain low power consumption and high speed. In Section 2, some existing full adder design is discussed. In Section 3, the proposed XOR XNOR cell full adder is discussed in detail. The results and performance of the proposed full adder are presented in section 4.

2.PREVIOUS WORKS

In recent years, various different logic designs have been introduced to implement 1 bit full adder circuit. The 1 bit full adders are divided into two structures such as static style and dynamic style. Static style full adders normally has more simple, low power consumed and stable structures compared to dynamic styles. The dynamic style full adders has some greatest advantages compared to static style like higher switching speed, less number of transistors, full swing voltage levels and no static power consumption. The area reduction was obtained from the PMOS network and also it reduces the capacitive load at the output node which reduces the delay.

Many research works combined both static and dynamic style and proposed hybrid dynamic static style.In all the literatures, so many variants of full adder structures are implemented. Each full adder's circuit has both advantages and disadvantages based on the technique used. All this structures tries to reduce the power delay product. Implementing full adder with conventional CMOS methods consumes more power, area and also delay. Based on XOR and XNOR cell, several designs are proposed in difference styles of logic. The pass transistor logic based full adder is designed, which reduces the power consumption. But the driving ability is limited.

The complimentary pass transistor logic dual rail structure designed with32 transistors and provides full swing output. The issue with the adder is high power consumption due to internal nodes and static inverter.

Transmission gate based 10 transistor full adder is consumes larger amount of power due to static inverters. There are lot more full adder structures are proposed to reduce power consumption, delay and area.Some of the full adder designs were discussed below.

1. Conventional Full Adder Design

The conventional CMOSbased full adder cell which is designed by using 28 transistors (28T) in the concept of PMOS pull up network and NMOS pull down network (Figure 1)for attaining the outputs carry and sum. This conventional CMOS can be suitable for low power consumption applications. But due to PMOS low mobility the overall speed of performance is reduced.

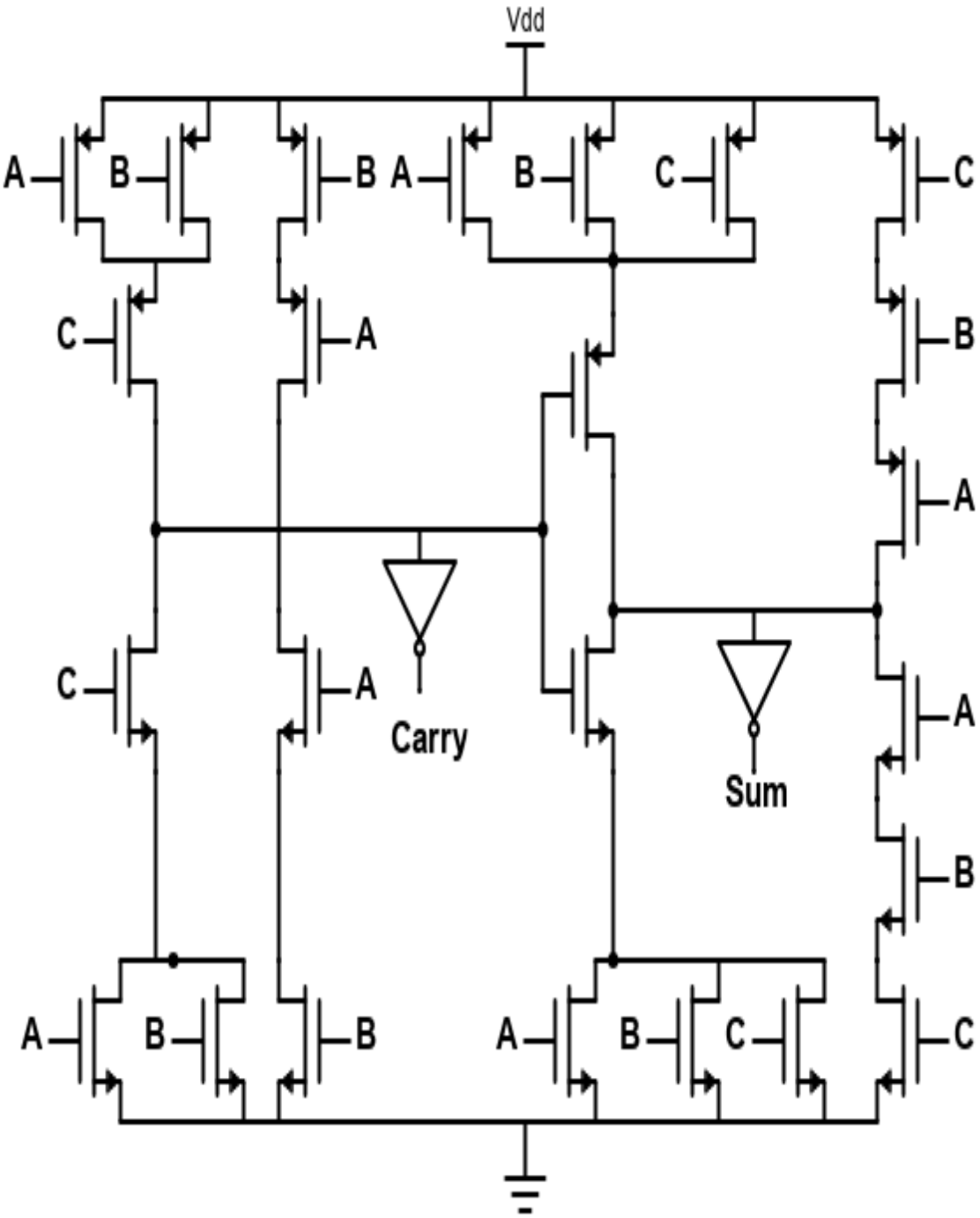

Figure 1. Conventional Complementary Metal Oxide Semiconductor Full Adder

2. XOR and XNORBased 22 Transistor Full Adder Design

The XOR / XNOR based 22 transistors full adder is shown in the figure 2.To generate the sum and carry the transmission gate based circuit is used. Due to TG design the circuit consumes large amount of power. But this22 Transistor consumes lower power compared when compared to 28 TransistorCMOS full adder.

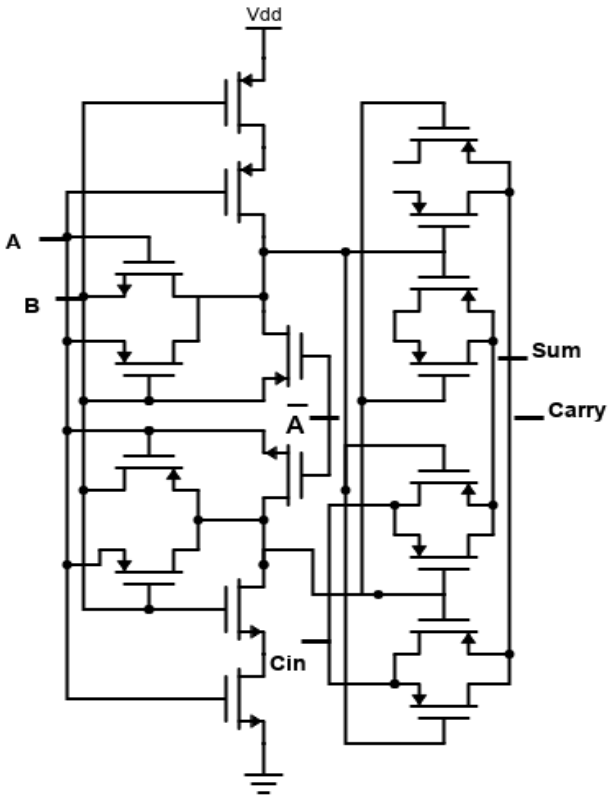

Figure 2. 22T XOR XNOR Full adder

3. XOR / XNOR Cell Based 18 Transistor Full Adder Design

The 18T based XOR -XNOR based full adder (Figure 3)simulation results are compared withconventional 28T full adder, which shows less power consumption.The problem with this full adder is output degradation during some input values. This degrades the entire performance of the full adder design.

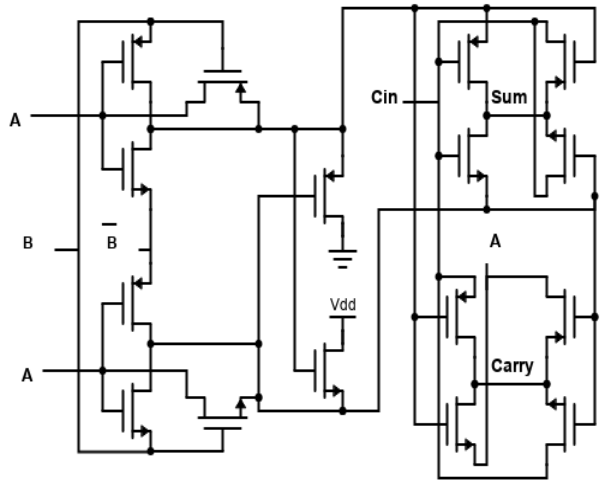

Figure3. 18T XOR XNOR Full adder

4. 14 T Full Adder

The 14T based full adder(Figure 4) is designed based on Low power XOR circuit and transmission gate. Due to usage of TG this leads high power consumption even though it has less power consumption when compared with Conventional Complementary Metal Oxide Semiconductor full adder.

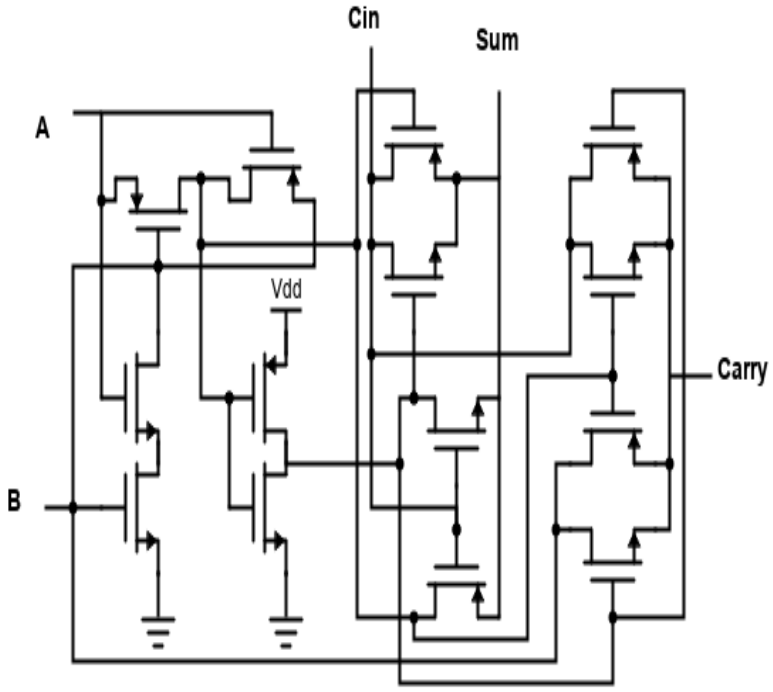

Figure 4. 14T XOR XNOR Full adder

5. Static Energy Recovery Full Adder

The Static energy recovery full adder(Figure 5)is designed with 10 transistors. Due to no direct path to ground, this full adder circuit consumes less power. This SERF(static energy recovery full adder**)**adderworks well in high voltages. But if the voltage level is scaled to lower, the circuit fails to attain the output levels and also has some threshold loss issues.

In the previous works (Figure 1 to figure 5), due to critical path delay the adder circuits high power consumption and delay is occurred. This work is concentrated to solve the critical path with the help of XOR XNOR cell structure

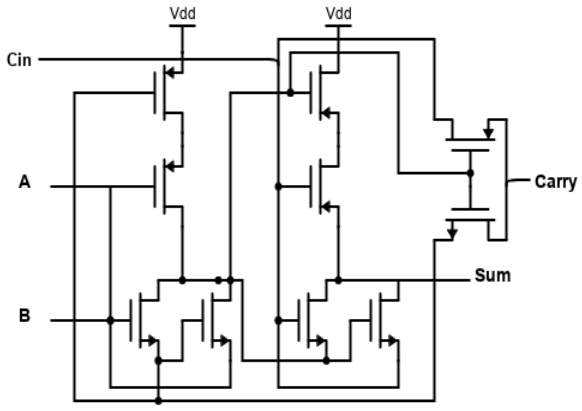

Figure 5. SERF Full Adder

I. Proposed Design:

XOR /XNOR Circuits

The XOR XNOR circuit is widely used in many full adder structures. This circuit is important block for circuits like adders, code converters, and odd parity checker, even parity checker to detect error and control the errors.

In these types of full adder structures, the main consumed power is by XOR XNOR block. Hence the designing of XOR XNOR block plays vital role in total power consumption in full adder design. Based on XOR XNOR block many hybrid adders are proposed and implemented.

The proposed XOR and XNOR cell based full adder is designedwith the negligible amount of power consumption.

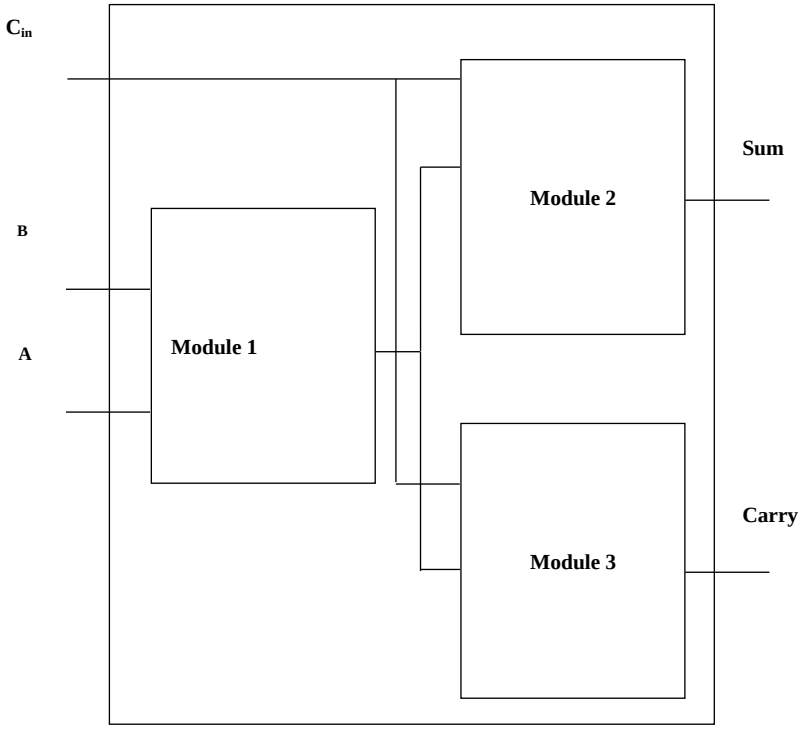

Figure 4: Functional Block Diagram

The Figure 4 shows the functional block diagram of the full adder structure. This structure is designed with three modules. Module 1 generates XOR and XNOR Logic. Likewise module 2 and Module 3 produces Sum and Carry outputs respectively.

The XOR and XNOR based Full adder is shown in the figure 6. This proposed XOR XNOR cell is constructed using 12 transistors is shown in figure 5.

This XOR XNOR cell is designed by merging the two proposed XOR and XNOR circuits and working in full swing mode for all the inputs of A and B. The critical path structure of any full adder circuit will consume more power and will maximize the delay of overall structure.

The longest path in a circuit is known for critical path which limits the speed of a circuit. In the proposed XOR and XNOR structure, there is no NOT gate for critical path selection. This is the main consideration for power and delay and also it is optimized by considering input capacitances of the structure is equal to zero.

By changing the inputs from 1 to 0 and vice versa in often makes glitches in circuits which dominate in power consumption. With less delay of this structure design, it reduces the glitches issue in the sum and carries generation stage.As already mentioned this XOR XNOR structure works in full swing, which allows good driving capability.

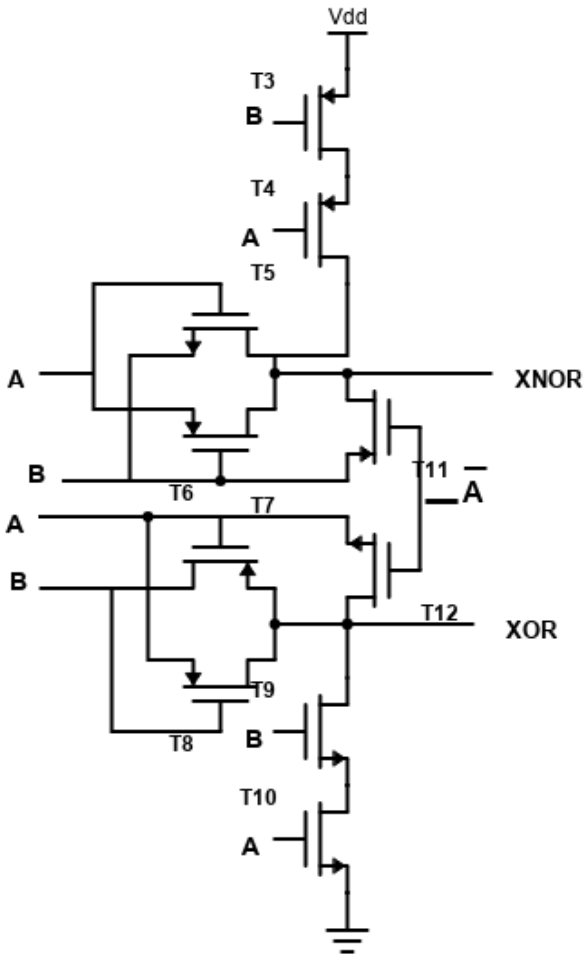

Figure 5. Proposed XOR and XNOR Structure

Generation of Sum and Carry Outputs:

Module 2 generates the sum output with the outputs of XOR cell and XNOR cell along with C_{in} input. So the equation (3) can be represented as in (5)

$$Sum = \overline{Cin}(A \oplus B) + Cin\ (A \odot B) \quad (5)$$

XOR output is multiplexed with inverted input of $C_{in}$and XNOR output is multiplexed with C_{in} to get sum output of Full adder.

Similarly the carry output is generated by Module 3 with the inputs Cin and B with the control of XNOR logic. Hence the equation (4) can be represented as in (6)

$$Cout = \overline{(A \odot B)}\ Cin + (A \odot B)B \quad (6)$$

XNOR inverted is multiplexed with C_{in} and XNOR is multiplexed with B input to get Carry output.

For instance, the inputs for A = 1, B = 1 C_{in}=0, transistor T3 and T4 are turned OFF. But the T5 and T6 NMOS Transistor become turned ON because of A and B inputs. This makes XNOR output as 1.

The XNOR output is inverted and multiplexed with Cin as well as B is multiplexed with XNOR. So this combination makes carry output as 1.

This inputs combination makes XOR Output as 0 by turning OFF the transistors T7 and T8. The sum output automatically turns into 0. This output is taken from the Figure 6.

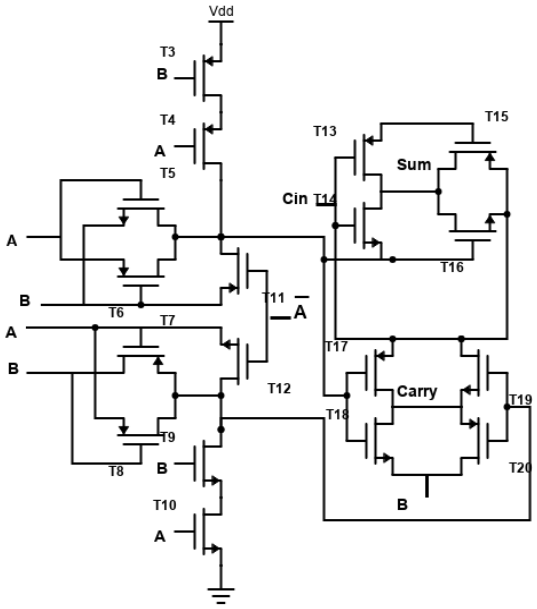

Figure 6. Proposed XOR and XNOR Based Full Adder

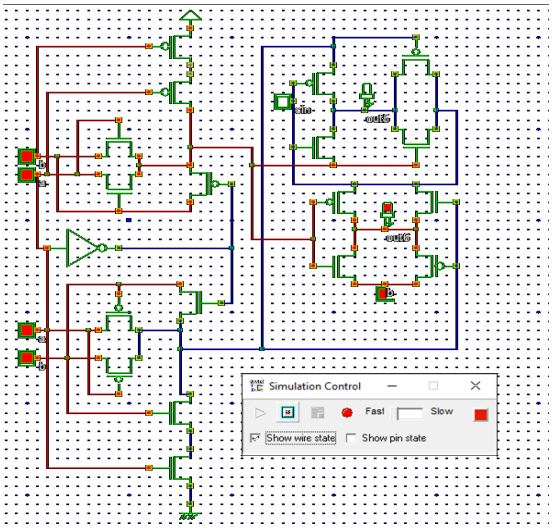

Figure 7. Output of PFA when A = 1, B = 1, Cin =0

Table 1 shows single bit full adder truth table.

Table I: General Truth Table of Full Adder

A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

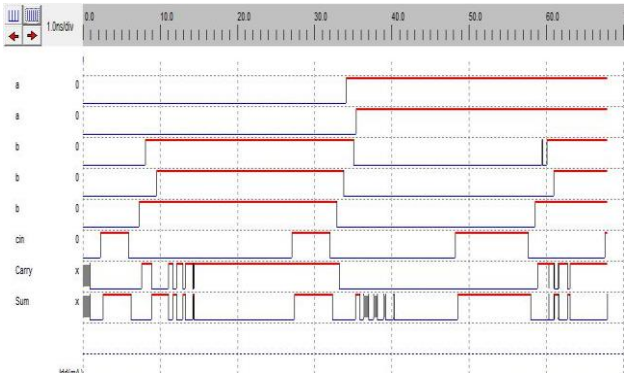

Figure 8. Simulation of PFA

Figure 7 illustrates the output of the proposed full adder when the inputs A=1, B=1 and Cin=0. Figure 8 shows the simulation result of proposed full adder in DSCH. With help of Verilog export from DSCH too, Verilog file is generated to obtain the layout design of proposed full adder design and figure 9 shows the layout design output of proposed full adder design using Microwind tool. The inputs and outputs of proposed full adder in layout design is shown in Figure 10.

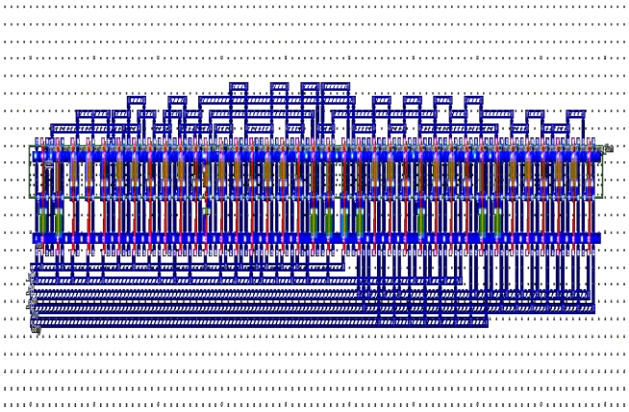

Figure 9. Layout forProposed Full Adder Circuit

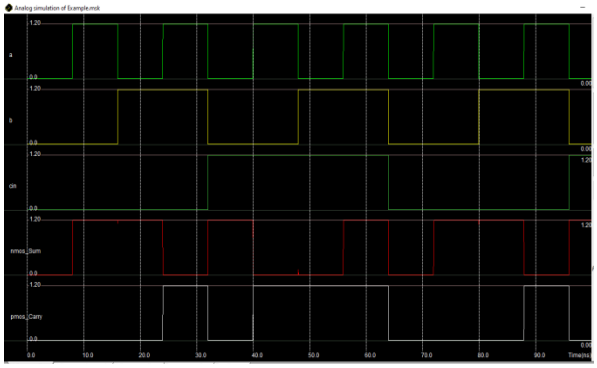

Figure 10. Layout simulation waveform of Proposed Full Adder

3.Results and Discussions

The simulation of the Conventional CMOS adder, 18T FA, 22T FA, 14T FA and SERF FA are carried out in 90nm, 65nm, 45nm, 35nm, 25nm, 18nm technologies using DSCH (Digital Schematic) and Microwind Tool.

Table II: Power analysis of full adder using various logic styles in 90nm Technology

Full Adder Design	Power (µW)
28T CMOS Conventional Adder	1600
18T Full Adder	926

22T Full Adder	550
14TT Full Adder	132
SERF Full Adder	513
Proposed Full Adder	84.99

Table III: Delay analysis of full adder using various logic styles in 90nm Technology

Full Adder Design	Delay (ps)
28T CMOS Conventional Adder	1548
18T Full Adder	11.75
22T Full Adder	6
14TT Full Adder	300.50
SERF Full Adder	13
Proposed Full Adder	5.23

Table IV: Power Analysis (μW) of various styles of full adders in different technologies

Designs	65nm	45nm	35nm	25nm	18nm
28T	895	512	52.185	19.42	4.648
18T	331	253	115	3.604	0.759
22T	291	124	18.382	8.537	2.325
14T	132	54.62	44.092	2.37	0.028
SERF	419	74.194	23.941	2.12	0.405
PFA	25.63	12.261	1.613	0.419	0.079

Table V: Delay (ps) analysis of various styles of full adders in different technologies

Designs	65nm	45nm	35nm	25nm	18nm
28T	1549	1640	1886	1686	1664
18T	16.20	217.20	109.20	52.40	43.40
22T	76	164.20	271.20	130.60	154.20
14T	300	335	384.50	769	206.30
SERF	14.20	91.80	230.20	451	82.20
PFA	74.60	36.40	50	32.80	29.80

Table VI: Transistor count comparison

Full Adder Design	Transistor Count
28T CMOS Conventional Adder	28
18T Full Adder	18
22T Full Adder	22
14TT Full Adder	14
SERF Full Adder	10
Proposed Full Adder	20

From the microwind tool, the delay within the interconnects can be defined as

$$Delay(in\ Sec) = 0.43 * R_L * C_L + 0.92\ (R * C_G + R_D * (C_L + C_G))$$

R_L= resistance of the line (in ohm)
C_L = capacitance of the interconnect (in Farad)
C_G = capacitance of the loading gates (in Farad)
R_D = CMOS device equivalent resistance of the driving the interconnect

Table II comparison shows the power consumption of different full adders with novel proposed full adder. The comparison shows that proposed a full adder consumes less power compared to other designs. Table III shows the delay comparison in 90nm technology. The power consumption and delay analysis of full adders are depicted in table IV and Table V.

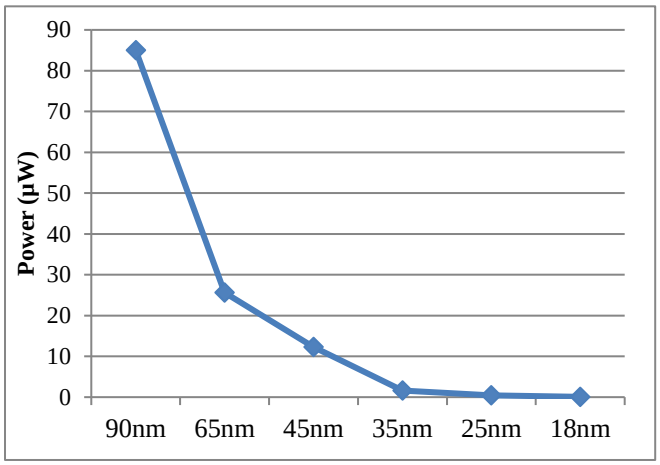

Figure 12: Power Consumption analysis of proposed full adder in different technologies

The proposed adder performance is compared with other full adder design in two methods. Since the PFA is based in XOR XNOR cell, its compared with other XOR XNOR cell based full adder and also its compared with non XOR XNOR based full adder design. The Figure 12 illustrates the proposed full adder in 90nm, 65nm, 45nm, 35nm, 25nm, 18nm technologies. The power consumption result of the full adder is in decreasing level when the technology size if reduced.

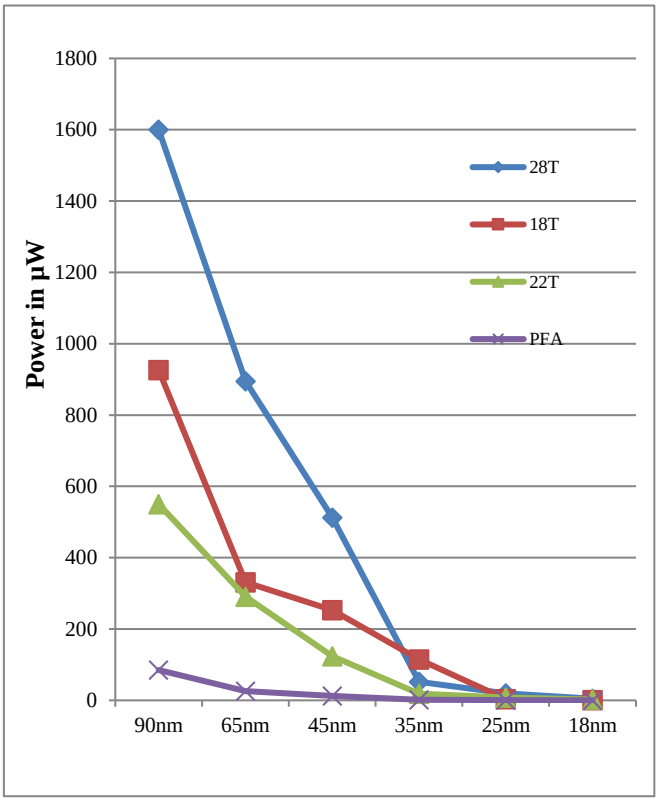

Figure 13: Power Comparison of XOR XNOR based Full Adders

Figure 13 shows the different power comparison of proposed adder in various nanometer technologies with 28T, 18T and 22T XOR XNOR based full adders. In both analysis, the proposed design shows low power consumption compared to all other compared full adders even the CMOS technology size is reduced.

Figure 14, compares the power analysis of proposed adder with non XOR XNOR base full adder with different nanometer technologies. In this comparison also the proposed full adder consumes less power.

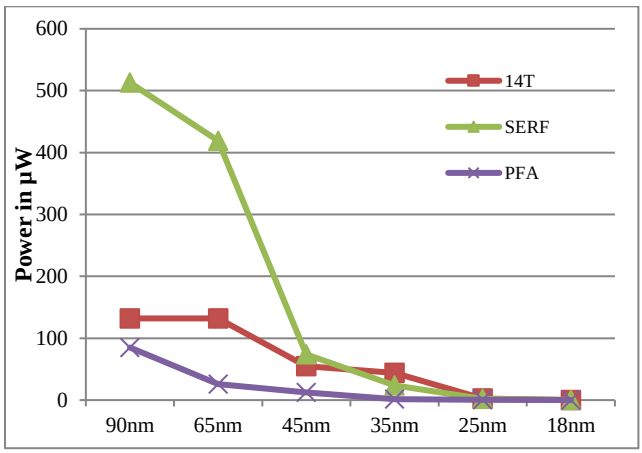

Figure 14: Power Comparison of different non XOR XNOR styles of Full Adders

From the simulation results analysis, the novel proposed full adder is consumes small amount of power compared to 28T CMOS conventional Adder, 18T FA, 22T FA, 14TT FA and SERF FA94.68%, 90.82%, 84.54%, 35.61% and 83.43% respectively.

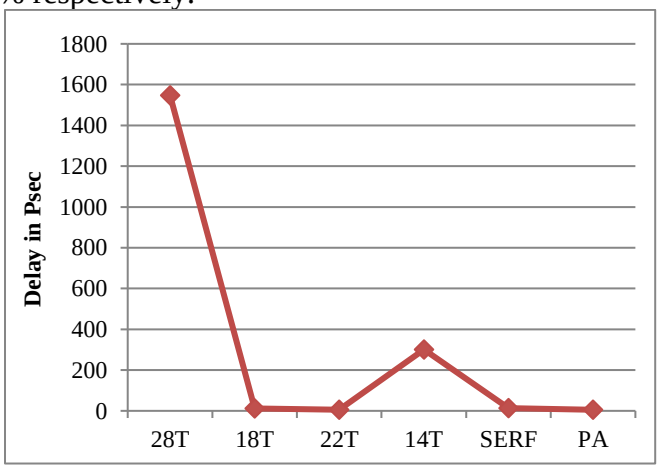

Figure 15: Delay analysis of various styles of full adders in 90nm

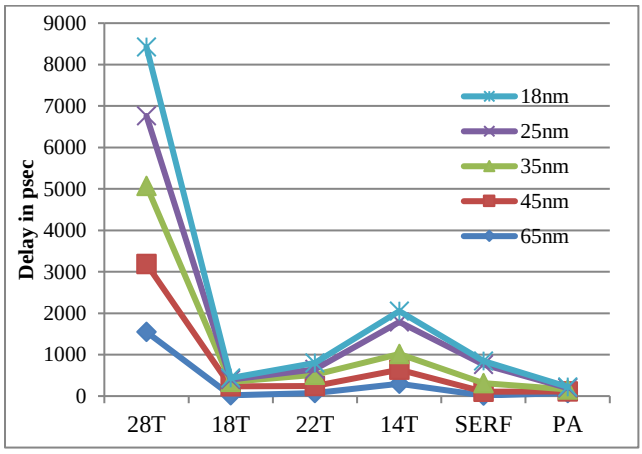

Figure 15: Delay analysis of various styles of full adders

From the figure 14 and figure 15 the delay analysis were carried out in similar way of power comparison analysis. The delay of the proposed adder is compared with 28T CMOS Conventional Adder, 18T FA, 22T FA, 14T FA and SERF FA in various complementary metal oxide semiconductortechnologies. The proposed adder has less delay with all other compared full adder designs.The figure16 depicts the number of transistors used in all the full adders considered in this work.

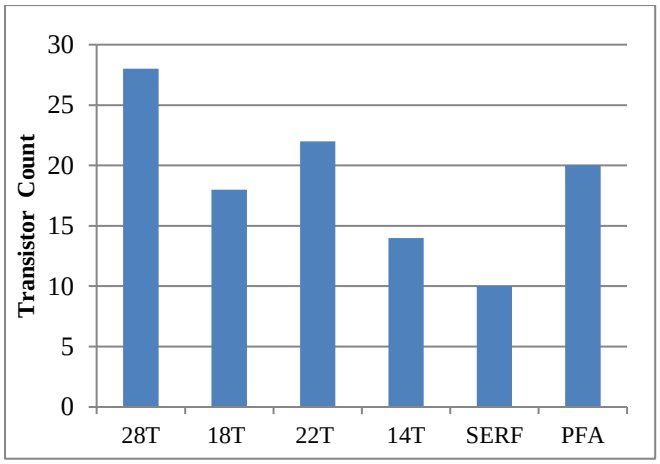

Figure 16: Transistor Count Analysis of various styles of full adder

4.CONCLUSION

In this work XOR XNOR cell structure based full adder is presented. The proposed full adder has less power consumption and less delay compared to other compared full adder circuit design because of the NOT gate is not used in the critical path and not using any feedback structure.The novel proposed XOR XNOR based full adder performance is compared withdifferent nanometer technologies on various types of full adder design to obtain the improved power consumption. The simulation were done using DSCH (Digital SCHmatic)and Microwind with different nanometre technologies and the results shows that proposed full adder produces good performance than all other design styles.The Proposed XOR XNOR Full adder consumes the power consumption 94.68%, 90.82%, 84.54%, 35.61% and 83.43% respectively, when compared to 28T CMOS Conventional Adder, 18T FA, 22T FA, 14TT FA and SERF FA and it can be suitable for low power VLSI arithmetic circuits, Internet of things such as smart appliances and robotic applications.Further the full adder can be designed using Multi Gate FinFETs for attaining furthermore improvement in performance of the adder.

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